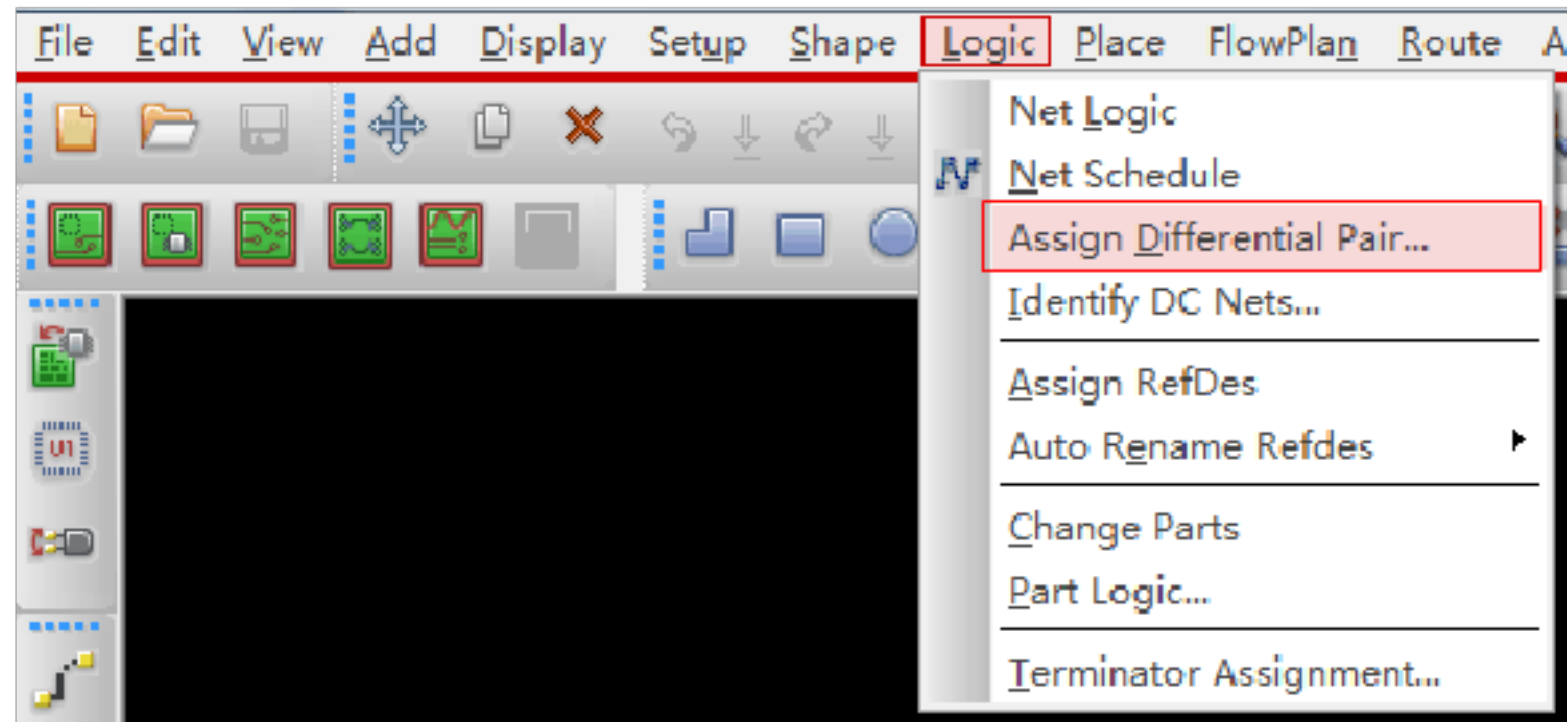


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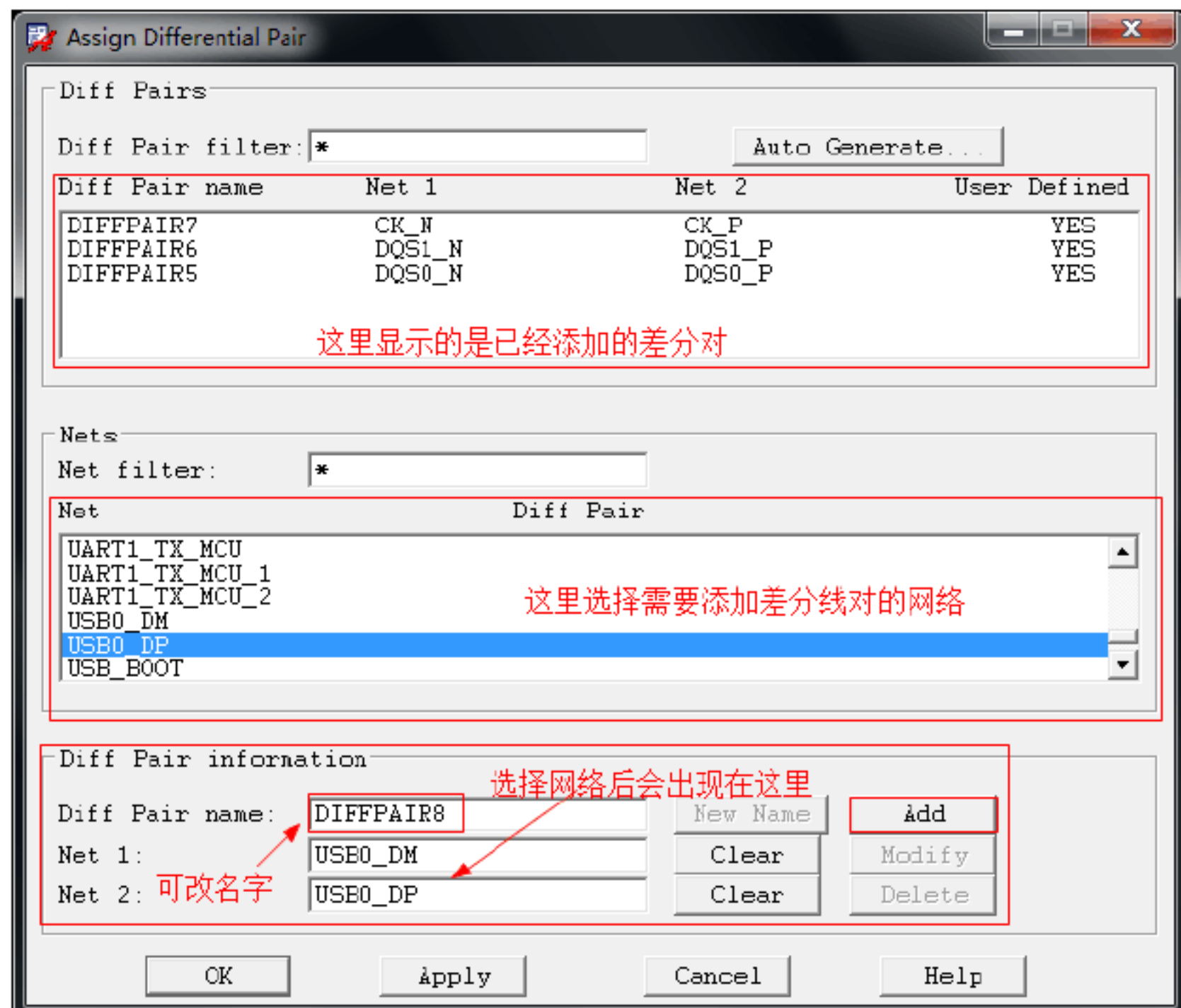
一、设置差分线的方法

方法一：

1、Logic→Assign Differential Pair



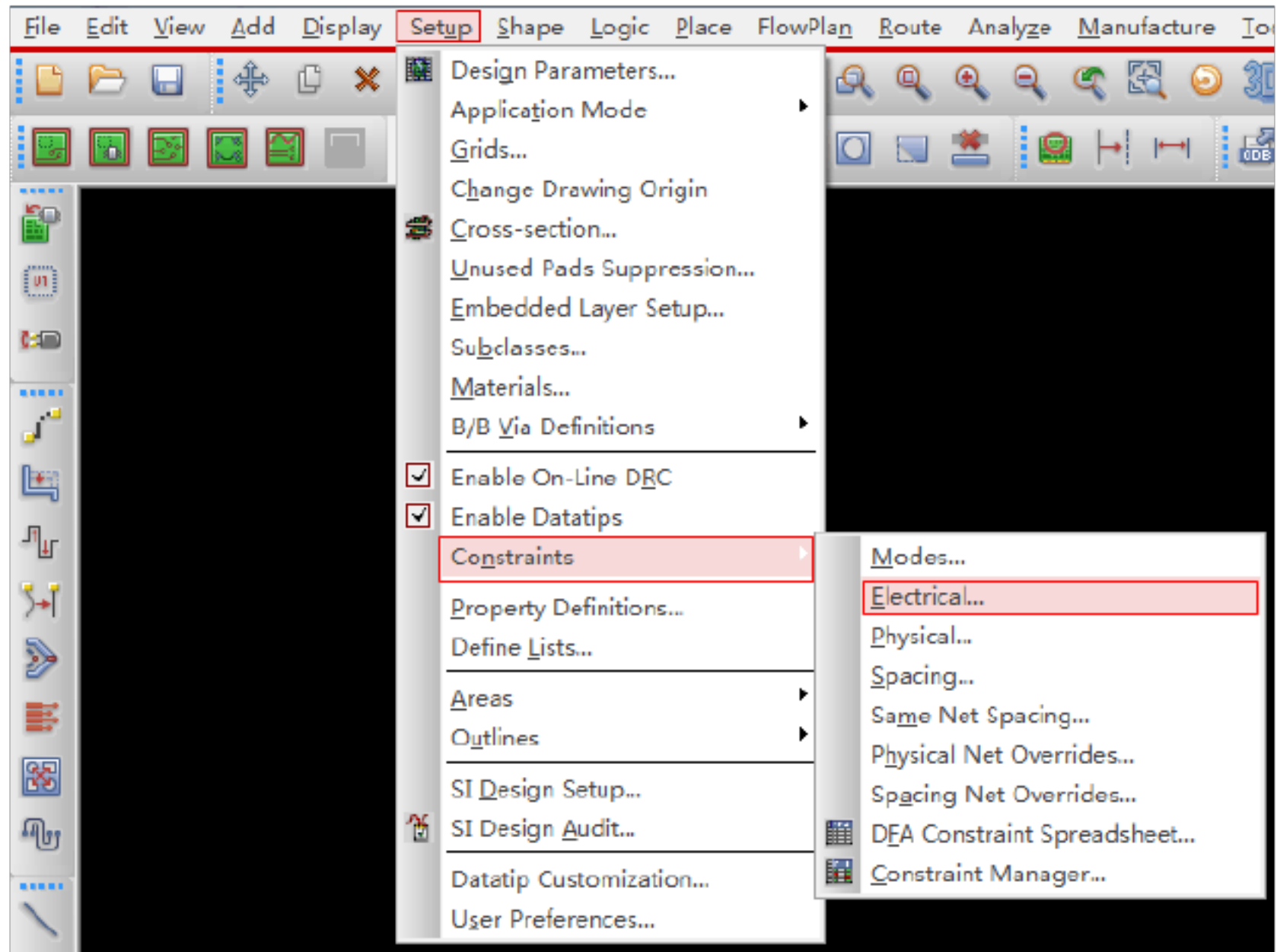
2、在弹出的对话框里选择需要添加的差分对，点击 Add 按钮，即可添加



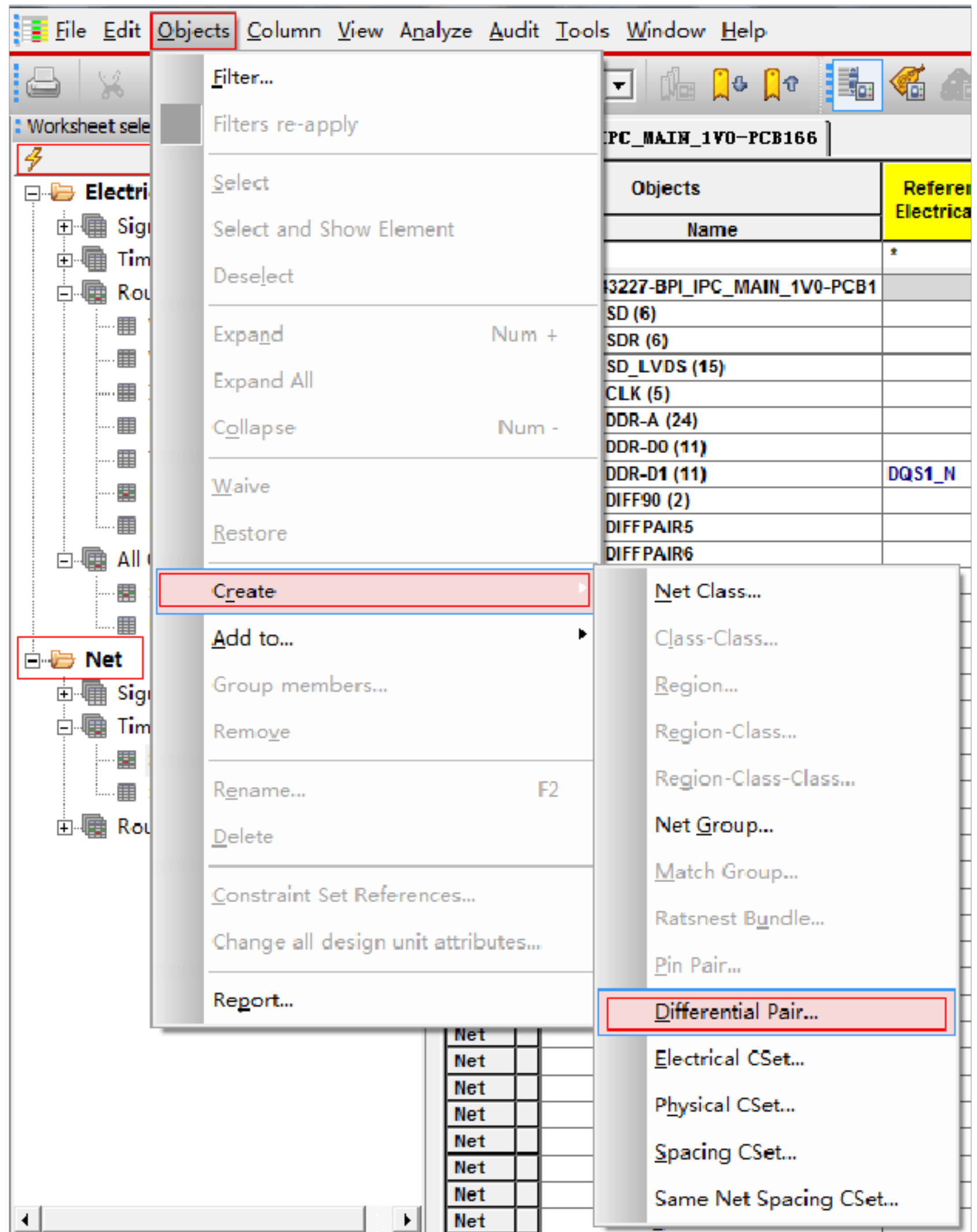
方法二：

1、Setup→Constraints→Electrical

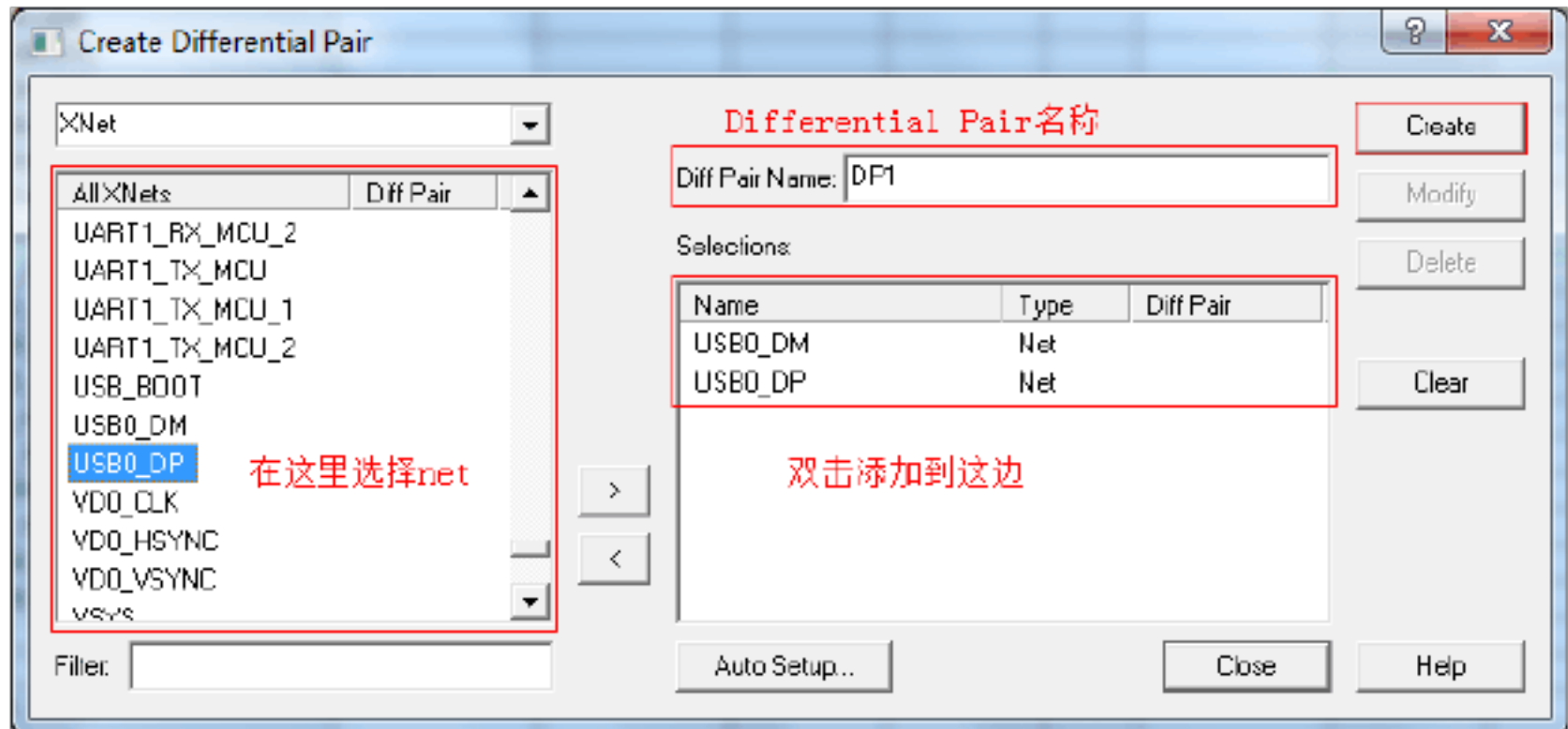
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2、选择 Net，然后在 Objects→Create→Differential Pair

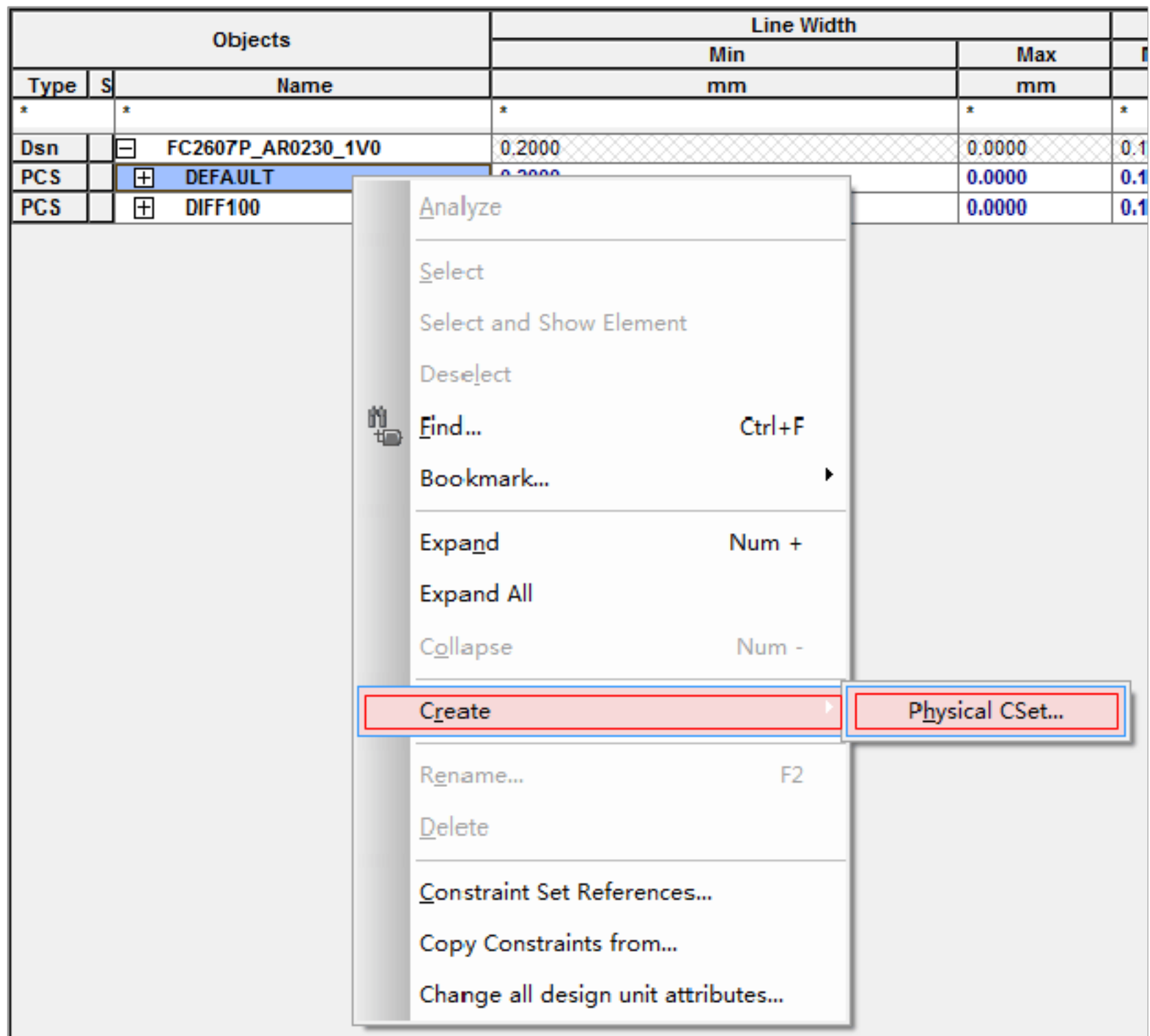


3、在弹出的对话框里选择需要添加的差分对，点击 Create 按钮，即可添加

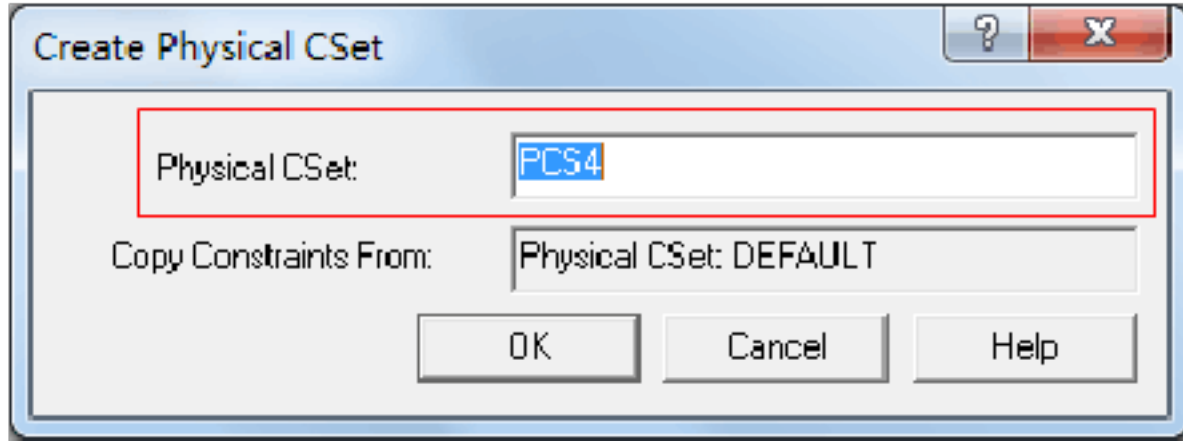


设置完差分线对后，需要设置其约束规则，方法如下：

- 1、初始默认的有一个 DEFAULT 规则，右击 DEFAULT，选择 Create→Physical CSet



- 2、弹出一对话框，在 Physical CSet 栏写上规则名称，建议根据差分线的阻抗描写，点击 OK，这里已经写好，规则名称为：DIFF100，就可以看到多了一行 PCS



| Objects | | |
|---------|--------------------------|--------------------|
| Type | S | Name |
| * | * | |
| Dsn | <input type="checkbox"/> | FC2607P_AR0230_1V0 |
| PCS | <input type="checkbox"/> | DEFAULT |
| PCS | <input type="checkbox"/> | DIFF100 |

3、设立好规则后就可以在这项规则里设置线宽间距等参数了

4、在 Net 一栏看到有已经设好的差分线，在 Referenced physical C Set 选项下选择刚刚设好的规则 DIFF100

| Objects | | | Referenced Physical CSet | Line Width |
|---------|--------------------------|--------------------|--------------------------|------------|
| Type | S | Name | | Min mm |
| * | * | | * | * |
| Dsn | <input type="checkbox"/> | FC2607P_AR0230_1V0 | DEFAULT | 0.2000 |
| DPr | <input type="checkbox"/> | LVDSCLK | DIFF100 | 0.1270 |
| DPr | <input type="checkbox"/> | LVDS0 | DEFAULT | 0.1270 |
| DPr | <input type="checkbox"/> | LVDS1 | DIFF100 | 0.1270 |
| DPr | <input type="checkbox"/> | LVDS2 | (Clear) | 0.1270 |
| DPr | <input type="checkbox"/> | LVDS3 | DIFF100 | 0.1270 |
| Net | | +3V3 | DEFAULT | 0.2000 |
| Net | | +5V | DEFAULT | 0.2000 |
| Net | | ADC_CH1 | DEFAULT | 0.2000 |
| Net | | AGND | DEFAULT | 0.2000 |

规则设置中各个项目的含义

Line Width (设置基本走线宽度)

Min: 最小线宽

Max: 最大线宽，写 0 相当于无限大

| Line Width | |
|------------|--------|
| Min mm | Max mm |
| * | * |
| 0.2000 | 0.0000 |
| 0.2000 | 0.0000 |
| 0.1270 | 0.0000 |

Neck (neck 模式，一般在间距很小的时候用到)

Min Width: 最小线宽

Max Length: 最大线长

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| Neck | |
|-----------|------------|
| Min Width | Max Length |
| mm | mm |
| * | * |
| 0.1270 | 0.0000 |
| 0.1270 | 0.0000 |
| 0.1270 | 0.0000 |

Differential Pair (差分线设置, 单端线可不写)

Min Line Spacing: 差分对的最小线间距

Primary Gap: 差分对理想线间距

Neck Gap: 差分对最小允许线间距

(+)Tolerance: 差分线允许的误差+

(-)Tolerance: 差分线允许的误差-

| Differential Pair | | | | |
|-------------------|-------------|----------|--------------|--------------|
| Min Line Spac | Primary Gap | Neck Gap | (+)Tolerance | (-)Tolerance |
| mm | mm | mm | mm | mm |
| * | * | * | * | * |
| 0.0000 | 0.0000 | 0.0000 | 0.0000 | 0.0000 |
| 0.0000 | 0.0000 | 0.0000 | 0.0000 | 0.0000 |
| 0.0000 | 0.1524 | 0.0000 | 0.0000 | 0.0000 |

Vias (过孔选择)

| Vias |
|-------------------|
| * |
| VIA8-BGA-FULL:VIA |
| VIA8-BGA-FULL:VIA |
| VIA8-BGA-FULL |

BB Via Stagger (设置埋/盲孔的过孔间距)

Min: 最小间距

Max: 最大间距

| BB Via Stagger | |
|----------------|--------|
| Min | Max |
| mm | mm |
| * | * |
| 0.1270 | 0.0000 |
| 0.1270 | 0.0000 |
| 0.1270 | 0.0000 |

Allow

Pad-Pad Connect: /

Etch: /

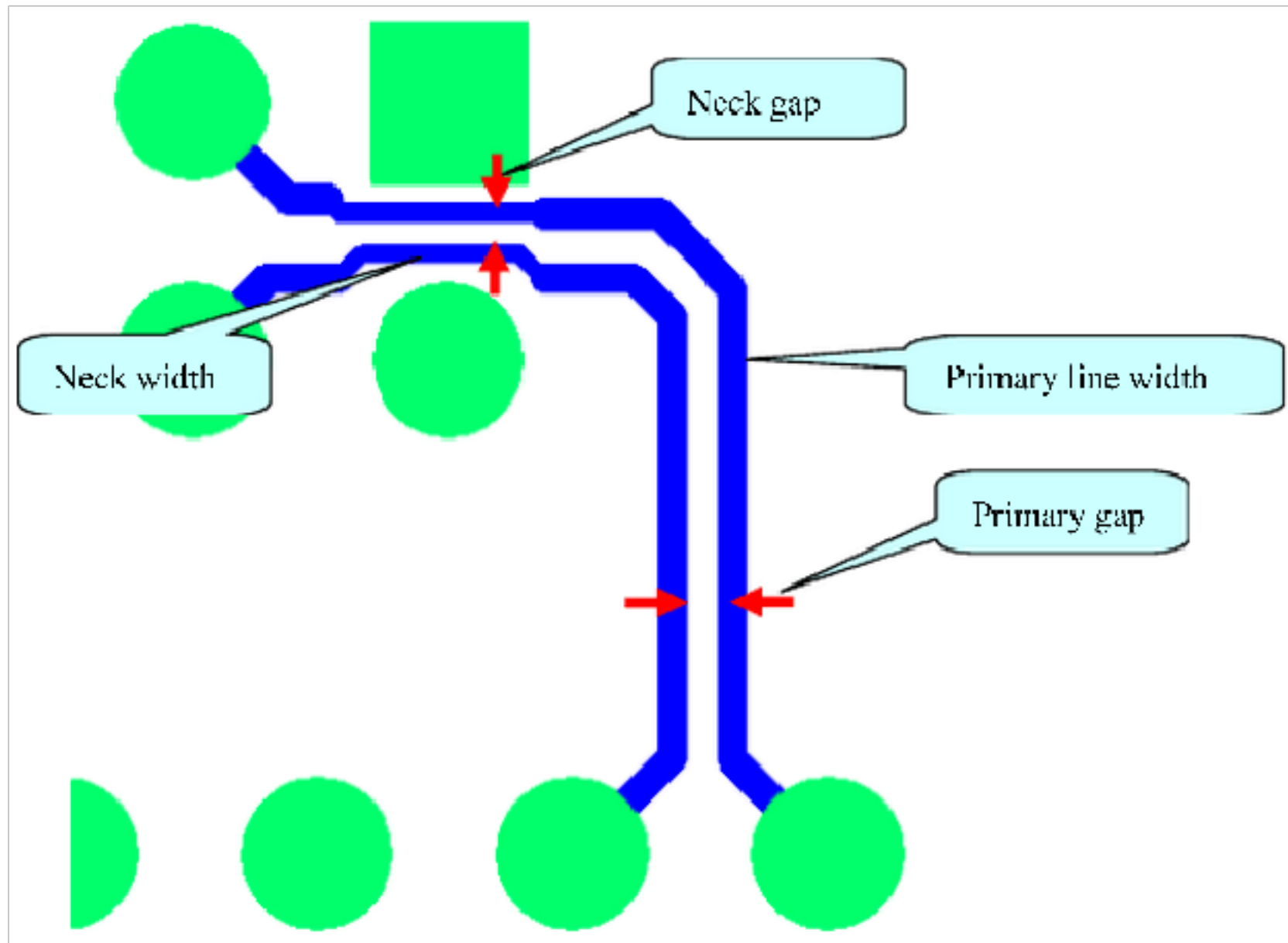
Ts: /

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| Allow | | |
|-----------------|------|----------|
| Pad-Pad Connect | Etch | Ts |
| * | * | * |
| ALL_ALLOWED | TRUE | ANYWHERE |
| ALL_ALLO... | TRUE | ANYWHERE |
| ALL_ALLO... | TRUE | ANYWHERE |

示意图:

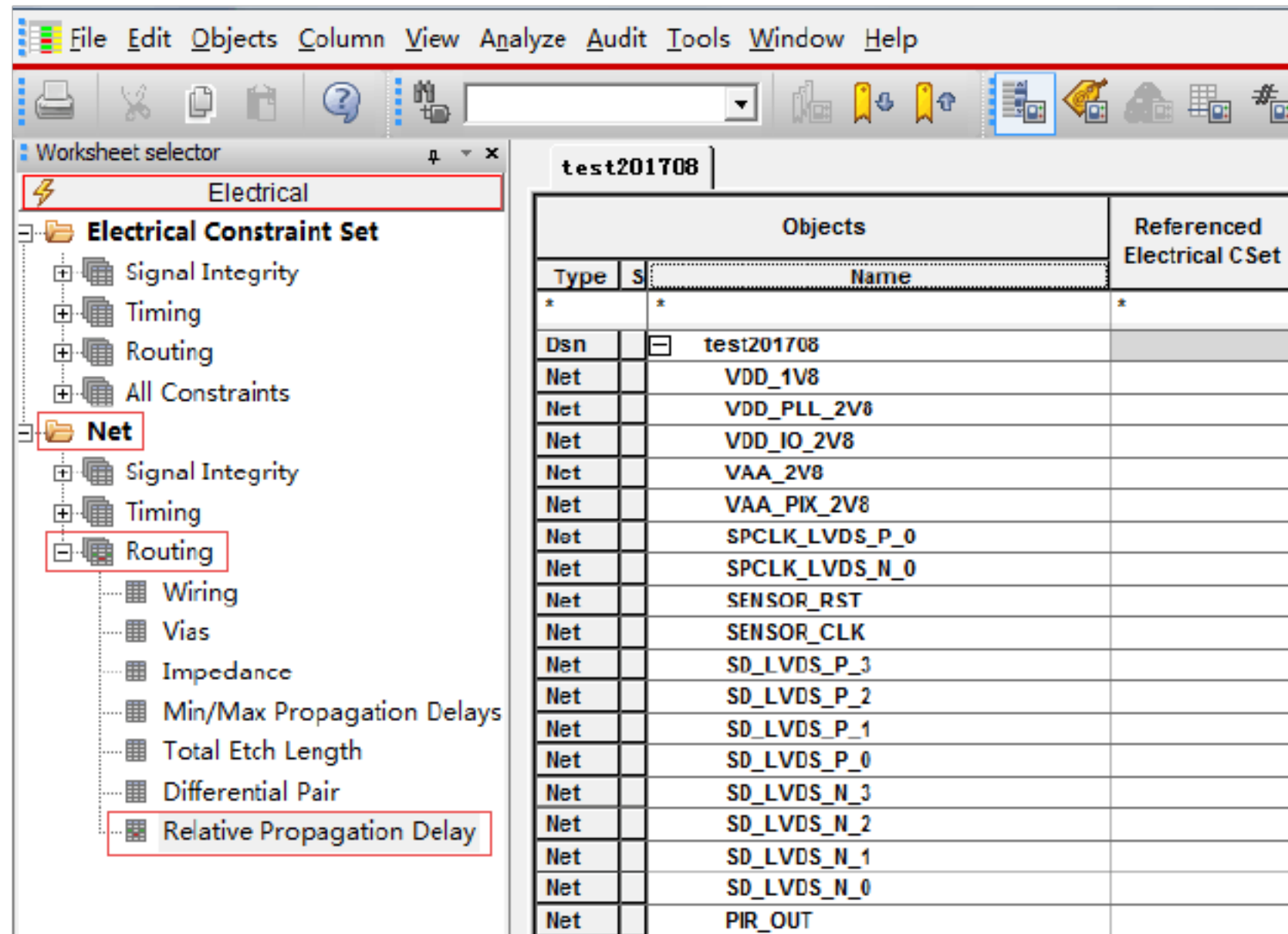


二、设置等长

1、进入规则设置页面

Electrical→Net→Routing→Relative Propagation Delay

大全



2、选中需要设置等长的网络，右击，选择 Create→Match Group

| Objects | | Referenced Electrical CSet | Pin Pairs | Pin Delay | |
|---------|----------------|----------------------------|-----------|-----------|-------|
| Type | S | | | Pin 1 | Pin 2 |
| Name | | | | mm | mm |
| Dsn | test201708 | | | | |
| Net | VDD_1V8 | | | | |
| Net | VDD_PLL_2V8 | | | | |
| Net | VDD_IO_2V8 | | | | |
| Net | VAA_2V8 | | | | |
| Net | VAA_PIX_2V8 | | | | |
| Net | SPCLK_LVDS_P_0 | | | | |
| Net | SPCLK_LVDS_N_0 | | | | |
| Net | SENSOR_RST | | | | |
| Net | SENSOR_CLK | | | | |
| Net | SD_LVDS_P_3 | | | | |
| Net | SD_LVDS_P_2 | | | | |
| Net | SD_LVDS_P_1 | | | | |
| Net | SD_LVDS_P_0 | | | | |
| Net | SD_LVDS_N_3 | | | | |
| Net | SD_LVDS_N_2 | | | | |
| Net | SD_LVDS_N_1 | | | | |
| Net | SD_LVDS_N_0 | | | | |
| Net | PIR_OUT | | | | |
| Net | N167783271 | | | | |
| Net | N16894797 | | | | |
| Net | N16864200 | | | | |
| Net | N16852014 | | | | |
| Net | N16845816 | | | | |
| Net | N16804061 | | | | |
| Net | N16804009 | | | | |
| Net | N16803976 | | | | |
| Net | N16803975 | | | | |
| Net | N16790184 | | | | |
| Net | N16790182 | | | | |
| Net | N16789963 | | | | |
| Net | N16789705 | | | | |
| Net | N16778964 | | | | |
| Net | N16778412 | | | | |
| Net | N16778268 | | | | |
| Net | N16778145 | | | | |
| Net | LED- | | | | |

Analyze

Select

Select and Show Element

Deselect

Find... Ctrl+F

Bookmark... ▶

Expand Num +

Expand All

Collapse Num -

Create ▶

Add to... ▶

Remove

Rename... F2

Delete

Constraint Set References...

SigXplorer...

Net Class...

Match Group...

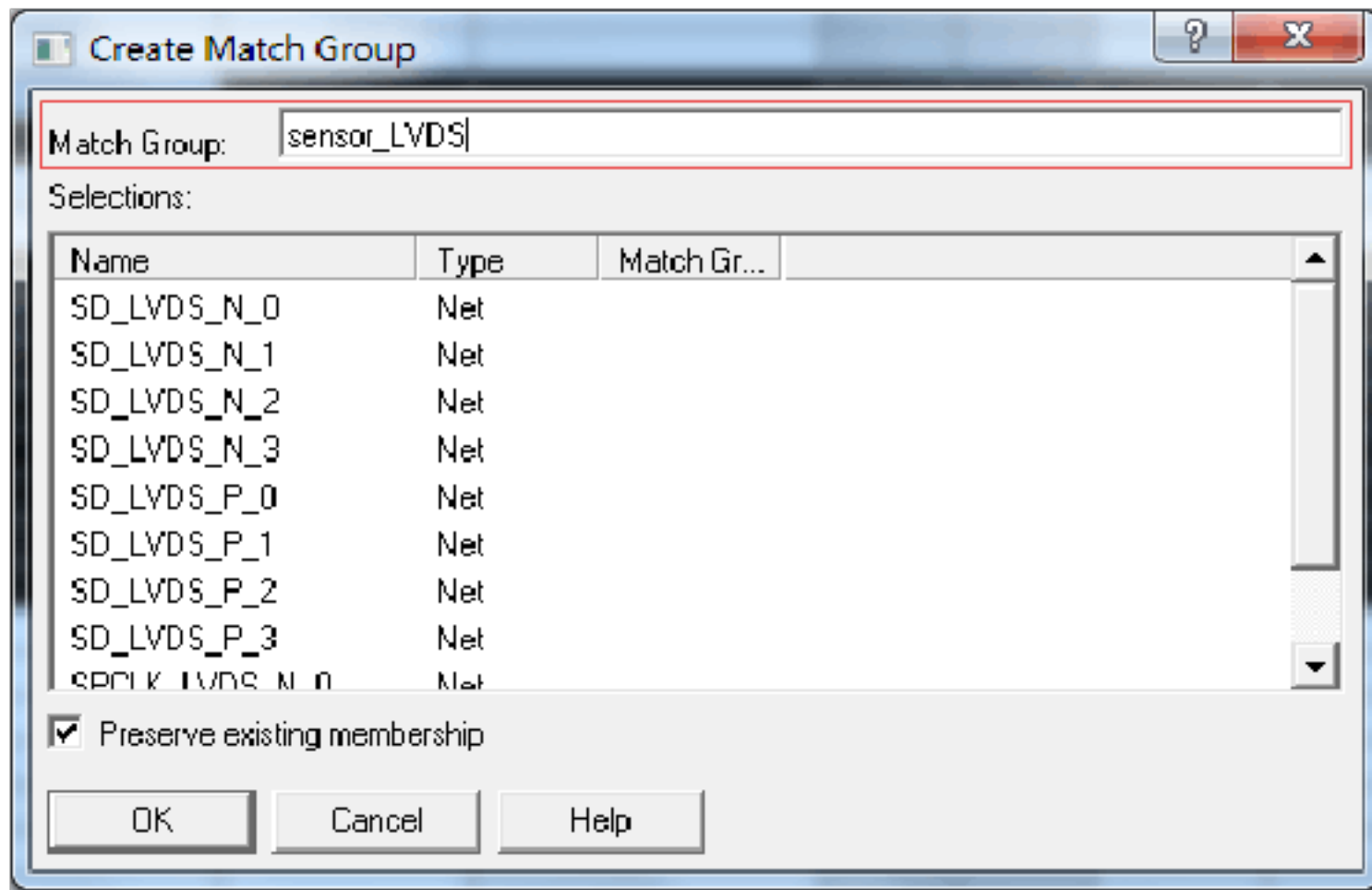
Net Group...

Pin Pair...

Differential Pair...

Electrical CSet...

3、更改组名称



4、设置好后，会显示 MGrp，如下图。这样等长的线组就设好了，接下来是设置等长的约束规则

| Objects | | Referenced Electrical CSet | Pin Pairs |
|---------|----------------------|----------------------------|---------------------------|
| Type | S | | |
| * | * | * | * |
| Dsn | [-] test201708 | | |
| MGrp | [-] SENSOR_LVDS (10) | | All Drivers/All Rece... |
| Net | SPCLK_LVDS_P_0 | | All Drivers/All Receivers |
| Net | SPCLK_LVDS_N_0 | | All Drivers/All Receivers |
| Net | SD_LVDS_P_3 | | All Drivers/All Receivers |
| Net | SD_LVDS_P_2 | | All Drivers/All Receivers |
| Net | SD_LVDS_P_1 | | All Drivers/All Receivers |
| Net | SD_LVDS_P_0 | | All Drivers/All Receivers |
| Net | SD_LVDS_N_3 | | All Drivers/All Receivers |
| Net | SD_LVDS_N_2 | | All Drivers/All Receivers |
| Net | SD_LVDS_N_1 | | All Drivers/All Receivers |
| Net | SD_LVDS_N_0 | | All Drivers/All Receivers |
| Net | VDD_1V8 | | |
| Net | VDD_PLL_2V8 | | |
| Net | VDD_IO_2V8 | | |

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