## 一、设置差分线的方法

方法一:

1, Logic→Assign Differenttial Pair



2、在弹出的对话框里选择需要添加的差分对,点击Add按钮,即可添加

7	/ Assig	in Differential Pair			
	Diff	Pairs			
	Diff	Pair filter:	*	Auto Gener	ate
	Diff	Pair name	Net 1	Net 2	User Defined
	DIFF DIFF DIFF	PAIR7 PAIR6 PAIR5	CK_N DQS1_N DQS0_N	CK_P DQS1_P DQS0_P	YES YES YES
			这里显示的是已经	S添加的差分对	
[	Nets				
	Net :	filter:	*		
	Net		Dif	ff Pair	
	UART UART UART USB( USB) USB	.1_TX_MCU [1_TX_MCU_1 [1_TX_MCU_2 ]_DM ]_DP BOOT	这	《里选择需要添加差分线对的	→ 列网络



方法二:

1、Setup→Constraints→Electrical



2、选择 Net, 然后在 Objects→Create→Differenttial Pair

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Worksheet s	ele	Filte	ers re-ap	ply				PC	_MAIN_1	¥0-P(	CB166		
<del>∮</del> ⊡-1∋ Elect	tri	<u>S</u> el	ect					F	Objects				Refere
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E T	im	Des	select					122	27 801 10	C 144	IN 41/0	DCP4	*
⊡ <b>!</b> ∰ R	OL	-						SD	(6)	C_MA	IN_1VV	-PGD1	
		Exp	a <u>n</u> d			Num	+	SD	R (6)				
		Exp	and All					SD.	_LVDS (18	5)			
						<b>N</b> 1			R-A (24)				
		Co	lapse			Num	-	DD	R-D0 (11)				
		Wa	ive					DD	R-D1 (11)				DQS1_N
			100					DIF	F90 (2)				
		Rea	store					DIF	FPAIR5				
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<b>↓</b>	► F	- 1	Net		
		- L		 -	

3、在弹出的对话框里选择需要添加的差分对,点击 Create 按钮,即可添加

1	Create Differential Pa	air							8	x
×Net -				Differenti		Create	6			
l	All×Nets	Diff Pair	•	l	Diff Pair Name: DP1				Modif	y I
	UART1_RX_MCU_2				Selections				Deleti	e
					Name LISPO DM		Туре Цан	Diff Pair		
	USB_BOOT	T1_TX_MCU_2 _BOOT D_DM _DP 在这里选择net >			USB0_DP		Net		Clear	
	USB0_DM USB0_DP 在这里 VD0_CLK VD0_HSYNC				双击添力	回到这边	2			
	Filter:		•		Auto Setup			Close	Нер	

设置完差分线对后,需要设置其约束规则,方法如下:

1、初始默认的有一个 DEFAULT 规则, 右击 DEFAU1T, 选择 Create→Physical CSet

Objects				Line Width	ı	
Objects				Min	Max	
Type S Name				mm	mm	
* *			*		*	*
Dsn E FC2607P_AR0230_	1V0		0.2000	******	0.0000	0.1
PCS		1	0.2000		0.0000	0.1
PCS I DIFF100		<u>A</u> nalyz	ze		0.0000	0.1
	ň	<u>S</u> elect Select Dese <u>l</u> e <u>F</u> ind	and Show Elen	nent Ctrl+F		
		Expan	id	Num +		
		Expan	nd All			
		C <u>o</u> llap	ose	Num -		
		C <u>r</u> eate	e	>	P <u>h</u> ysical CSet	



2、弹出一下对话框,在 Physical CSet 栏写上规则名称,建议根据差分线的阻抗描写,点击 OK,这里已经写好,规则名称为: DIFF100,就可以看到多了一行 PCS

Create Physical CSet		? ×
Physical CSet:	PCS4	
Copy Constraints From:	Physical CSet: DEFAULT	
	OK Cancel	Help

Objects									
Туре	S		Name						
*		*							
Dsn			FC2607P_AR0230_1V0						
PCS		Ŧ	DEFAULT						
PCS		+	DIFF100						

3、设立好规则后就可以在这项规则里设置线宽间距等参数了

4、在Net一栏看到有已经设好的差分线,在Referenced physical C Set 选项下选择刚刚 设好的规则 DIFF100

4 Electrical					
2 Discission			Objecto	Defense	Line V
+ft Physical			objects	Referenced	Min
📮 🦢 Physical Constraint Set	Type S		Name	Physical Coet	mm
	*		ż	*	*
By Layer	Dsn		FC2607P_AR0230_1V0	DEFAULT	0.2000
	DPr		EVDSCLK	DIFF100 👻	0.1270
	DPr		+ LVDS0	DEFAULT	0.1270
	DPr		1 LVDS1	DIFF100	0.1270
🖻 🥪 Region	DPr		LVDS2	(Clear)	0.1270
All Layers	DPr		E LVDS3	DIFF100	0.1270
1000 C	Net		+3V3	DEFAULT	0.2000
	Net	Π	+5V	DEFAULT	0.2000
	Net		ADC_CH1	DEFAULT	0.2000
	Net		AGND	DEFAULT	0.2000

### \*规则设置中各个项目的含义\*

Line Width (设置基本走线宽度)

Min: 最小线宽

Max: 最大线宽, 写0相当于无限大

Line Width					
Min	Max				
mm	mm				
ž	*				
0.2000	0.0000				
0.2000	0.0000				
0.1270	0.0000				

Neck (neck 模式,一般在间距很小的时候用到)

Min Width: 最小线宽

Max Length: 最大线长

Neck				
Min Width	Max Length			
mm	mm			
*	*			
0.1270	0.0000			
0.1270	0.0000			
0.1270	0.0000			

Differential Pair (差分线设置,单端线可不写)

Min Line Spacing: 差分对的最小线间距

Primary Gap: 差分对理想线间距

Neck Gap: 差分对最小允许线间距

(+) Tolerance: 差分线允许的误差+

(-)Tolerance: 差分线允许的误差-

Differential Pair									
Min Line Spac Primary Gap		Neck Gap	(+)Tolerance	(-)Tolerance					
mm	mm	mm	mm	mm					
*	*	*	*	*					
0.0000	0.0000	0.0000	0.0000	0.0000					
0.0000	0.0000	0.0000	0.0000	0.0000					
0.0000	0.1524	0.0000	0.0000	0.0000					

Vias (过孔选择)

Vias	-
*	[
VIA8-BGA-FULL:VIA	ŝ
VIA8-BGA-FULL:VIA	
VIA8-BGA-FULL	

BB Via Stagger (设置埋/盲孔的过孔间距)

Min: 最小间距

Max: 最大间距

BB Via Stagger

Min	Max		
mm	mm		
×	*		
0.1270	0.0000		
0.1270	0.0000		
0.1270	0.0000		

### Allow

Pad-Pad Connect: /

Etch: /

Ts: /

Allow					
Pad-Pad Connect	Etch	Ts			
×	*	ż			
ALL_ALLOWED	TRUE	ANYWHERE			
ALL_ALLO	TRUE	ANYWHERE			
ALL_ALLO	TRUE	ANYWHERE			

示意图:



# 二、设置等长

## 1、进入规则设置页面

 $Electrical \rightarrow Net \rightarrow Routing \rightarrow Relative Propagation Delay$ 

File Edit Objects Column View Analyze Audit Tools Window Help						
🗕 % й 🛍 🎱 🖫 🗖		🔽 🎼 🎝 🎝 🖬 🗲	<b>A</b> 🖥 掩			
🕯 Worksheet selector 🛛 📮 👻 🗙	test201708					
🗲 Electrical						
Electrical Constraint Set		Referenced				
🗈 🖷 Signal Integrity	Туре	s Name	Electrical Coet			
⊡ 🗐 Timing	*	*	*			
E Bouting	Dsn	e test201708				
	Net	VDD_1V8				
	Net	VDD_PLL_2V8				
∃ 😓 Net	Net	VDD_IO_2V8				
🗄 🖩 Signal Integrity	Net	VAA_2V8				
🕀 📠 Timing	Net	VAA_PIX_2V8				
E Bouting	Net	SPCLK_LVDS_P_0				
	Net	SPCLK_LVDS_N_0				
Wiring	Net	SENSOR_RST				
Vias	Net	SENSOR_CLK				
Impedance	Net	SD_LVDS_P_3				
Min/Max Propagation Delays	Net	SD_LVDS_P_2				
	Net	SD_LVDS_P_1				
	Net	SD_LVDS_P_0				
Differential Pair	Net	SD_LVDS_N_3				
	Net	SD_LVDS_N_2				
	Net	SD_LVDS_N_1				
	Net	SD_LVDS_N_0				
	Net	PIR_OUT				

2、选中需要设置等长的网络,右击,选择 Create→Match Group

Objects				Deferenced			Pin Delay		Τ	
	Objects				Flectrical CSet	Pin Pairs		Pin 1	Pin 2	
Туре	S	Name			Lieurical e set			mm	mm	
*		ż			*	*		*	*	*
Dsn		test201708								
Net		VDD_1V8								8
Net		VDD_PLL_2V8								8
Net		VDD_IO_2V8								8
Net		VAA_2V8								8
Net		VAA_PIX_2V8								8
Net		SPCLK_LVDS_P_0								
Net		SPCLK_LVDS_N_0		Analyz	e					
Net		SENSOR_RST								8
Net		SENSOR_CLK		<u>S</u> elect						88
Net		SD_LVDS_P_3		Colort	and Chaw Elana					
Net		SD_LVDS_P_2		Select	and show clem	ent				
Net		SD_LVDS_P_1		Desele	ect					
Net		SD_LVDS_P_0								
Net		SD_LVDS_N_3	11	<u>F</u> ind		Ctrl+F				
Net		SD_LVDS_N_2								
Net		SD_LVDS_N_1	Bookmark							
Net		SD_LVDS_N_0								
Net		PIR_OUT		Expan	d	Num +				8
Net		N167783271								8
Net		N16894797		Expan	d All					8
Net		N16864200		Collanse Num -		Nuss				8
Net		N16852014		Conap	50	Num -				8
Net		N16845816		<u> </u>						1
Net		N16804061		C <u>r</u> eate	•		Net	<u>C</u> lass		
Net		N16804009		Add to		•	Mate	-h Grour	、 、	
Net		N16803976		<u>A</u> uu to	/		Indu	in oroup	/	
Net		N16803975		Remov	/e		Net	Group		
Net		N16790184								
Net		N16790182		Renam	1e	F2	<u>P</u> in P	Pair		
Net		N16789963					D.10	1.10		
Net		N16789705		<u>D</u> elete			Diffe	rential P	air	
Net		N16778964					Elect	rical CSe	et	
Net		N16778412		Constraint Set References			Lieu	incar cot		
Net		N16778268								12
Net		N16778145		SigXplorer						18
Net		LED-		sig <u>∧</u> piorer						8
			_			Y Y Y Y Y Y Y Y				

3、更改组名称

1	Create Match Group		<u>१</u> - २	٢
	Match Group: sensor_L	/DS		
l	Selections:			
	Name	Туре	Match Gr	•
	SD_LVDS_N_0	Net		
	SD_LVDS_N_1	Net		
	SD_LVDS_N_2	Net		
	SD_LVDS_N_3	Net		
	SD_LVDS_P_0	Net		
	SD_LVDS_P_1	Net		
	SD_LVDS_P_2	Net		
	SD_LVDS_P_3	Net		_1
		Nət		<u> </u>
	Preserve existing member	ership		
	OK Cance	<u> </u>	Help	

## 4、设置好后,会显示 MGrp,如下图。这样等长的线组就设好了,接下来是设置等长的约束

规则

		Objects	Referenced	Pin Pairs		
Туре	S	Name	Electrical elect			
*	* *		*	*		
Dsn		E test201708				
MGrp		SENSOR_LVDS (10)		All Drivers/All Rece		
Net		SPCLK_LVDS_P_0		All Drivers/All Receivers		
Net		SPCLK_LVDS_N_0		All Drivers/All Receivers		
Net		SD_LVDS_P_3		All Drivers/All Receivers		
Net		SD_LVDS_P_2		All Drivers/All Receivers		
Net Net		SD_LVDS_P_1		All Drivers/All Receivers		
		SD_LVDS_P_0		All Drivers/All Receivers		
Net		SD_LVDS_N_3		All Drivers/All Receivers		
Net		SD_LVDS_N_2		All Drivers/All Receivers		
Net		SD_LVDS_N_1		All Drivers/All Receivers		
Net		SD_LVDS_N_0		All Drivers/All Receivers		
Net		VDD_1V8				
Net		VDD_PLL_2V8				
Net		1/DD IO 21/8		000000000000000000000000000000000000000		



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