Quad Universal Asynchronous Receiver/Transmitter (UART)
with FIFO's

Description

The IMP16C554 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5MHz.

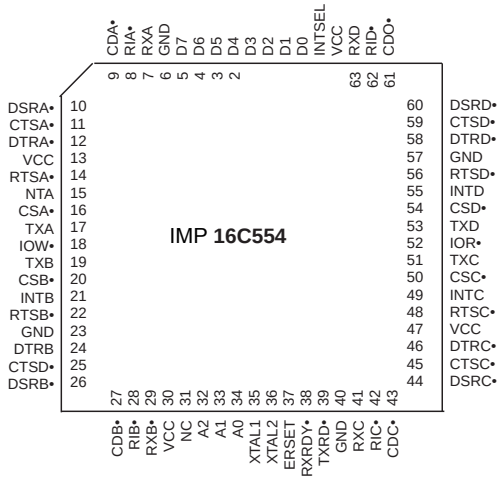
The IMP16C554 is an improved version of the IMP16C550 UART with higher operating speed and lower access time. The IMP16C554 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The IMP16C554 provides internal loop-back capability for on board diagnostic testing.

The IMP16C554 is fabricated in an advanced 1.2u CMOS process to achieve low drain power and high speed requirements.

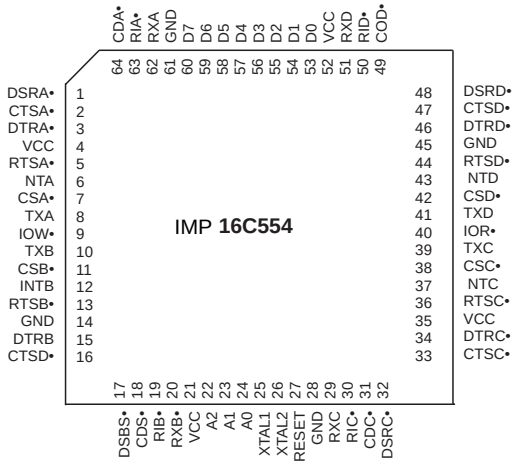
Key Features

- 16 byte receive FIFO with error flags
- Modem control signal (CTS*, RTS*, DSR*, DTR*, RI* ,CD*)
- Programmable character lengths(5,6,7,8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TLL compatible inputs. outputs
- Software compatible with Ei8250, 1Ei16C550
- 460.8kHz transmit/receive operation with 7.372 MHz crystal or external clock source

Pin Configuration



68-PIN PLCC



64-PIN QFP

408-432-9100/www.impweb.com

SYMBOL DESCRIPTION

symbol	pin	Signal Type	Pin Description
D0-D7	5-66	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. Do is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7.29 41.63	I	Serial data input. The serial information (data) received from serial port to IMP16C554 receive input circuit . A mark (high) is logic one and a space (low)is logic zero. During the local loopback mode the RX input is disabled from external connection and to the TX output internally.
TX A-B TX C-D	17.19 51.53	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark(high) state during reset, local loopback mode or when the transmitter is disabled.
CS*A-B CS*C-D	16.20 50.54	I	Chip select. (active low) A low at this pin enables the IMP16C554/CPU data transfer operation. Each UART sections of the IMP16C554 can be accessed independently.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2 or buffered clock output. See XTAL1.
LOW*	18	I	Write strobe.(active low)A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6.23 40.57	O	Signal and power ground.
IOR*	52	I	Read strobe.(active low)A low level on this pin transfers the contents of the IMP16C554 data bus to the CPU.

SYMBOL DESCRIPTION

symbol	pin	Signal Type	Pin Description
TXRDY*	39	O	Transmit ready. (active low) This pin goes high when the transmit FIFO of the IMP16C554 is full. It can be used as a single or multi-transfer.
A2	32	I	Address select line 2.To select internal registers.
A1	33	I	Address select line 1.To select internal registers.
A0	34	I	Address select line 0.To select internal registers.
RXRDY*	38	O	Receive ready.(active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
INTSEL	65	I	Interrupt type select. Enable /disable the interrupt three state function. Normal interrupt output can be selected by connecting this pin to VCC(MCR bit-3 does not have any effect on the interrupt output).The three state interrupt output is selected when this pin is left open or connected to GND and MCR bit-3 is to “1”.
INT A-B INT C-D	15.21 49.55	O	Interrupt output.(active high) this pin goes high (when enable by the interrupt enable register)whenever a receiver error. receiver data available. transmitter empty, or modem status condition flag is detected.
RTS*A-B RTS*C-D	14.22 48.56	O	Request to send.(active low) To indicate that the transmitter has data ready to send .Writing a “1” in the modem control register(MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*A-B DTR*C-D	12.24 46.58	O	Data terminal ready. (active low) To indicate that IMP16C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0).writing a “1” at the MCR bit-0 will set the DTR* output to low.

SYMBOL DESCRIPTION

symbol	pin	Signal Type	Pin Description
			This pin will be set to high state after writing a “0” to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	37	I	Master reset.(active high)A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*A-B CTS*C-D	11.25 45.59	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*A-B DSR*C-D	10.26 44.60	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*A-B CD*C-D	9.27 43.61	I	Carrier detect.(active low) A low on this pin indicates the carrier has been detected by the modem.
RI*A-B RI*C-D	8.28 42.62	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13.30 47.64	I	Power supply input.

IMP16C554 ACCESSIBLE REGISTERS

A2A1A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	Modem status interrupt	Receive line status interrupt	Transmit holding register	Receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA Mode select	XMITFIFO reset	RCVRFIFO reset	FIFO enable
0 1 0	ISR	0/FIFOs enabled	0/FIFOs enabled	0	0	int priority bit-2	Int priority bit-1	Int priority bit-0	Int status
0 1 1	LCR	Divisor latch enable	Set break	Set parity	Even parity	Parity enable	Stop bits	Word length bit-1	Word length bit-0
1 0 0	MCR	0	0	0	Loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	o/FIFO error	trans empty	trans holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to “1”.