26 W BTL and 2 × 13 W SE or 4 × 13 W SE power amplifier

TDA8512J

CONTENTS

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1 FEATURES

- Requires very few external components
- High output power
- Low output offset voltage Bridge-Tied Load (BTL) channel
- Fixed gain
- Good ripple rejection
- Mode select switch: operating, mute and standby
- Short-circuit safe to ground and across load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on and switch-off plops
- Flexible leads
- Low thermal resistance
- Identical inputs: inverting and non-inverting.

2 APPLICATIONS

- Multimedia systems
- Active speaker systems (stere with sub woofer or QUAD).

3 GENERAL DESCR PTION

The TDA8512J is an tegrated class-B output amplifier in a 17-lead Single-In-Line SIL) power package. It contains 4 × 13 W Single Ended (SE) amplifiers of which two can be used to con gure a 26 W BTL amplifier.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	ONDIT ONS	MIN.	TYP.	MAX.	UNIT
General						
V_P	supply voltage		6	15	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	80		mA
I_{stb}	standby current		–	0.1	100.0	µA
BTL channel						
P_o	output power	R_L = 4 Ω; THD = 10%	–	26	–	W
SVRR	supply voltage ripple rejecti n		46	–	–	dB
$V_{n(o)}$	noise output voltage	R_S = 0 Ω	–	70	–	µV
$\|Z_i\|$	input impedance		25	–	–	kΩ
$\|\Delta V_{OO}\|$	DC output offse voltage		–	–	150	mV
SE channels						
P_o	output power	THD = 10%				
		R_L = 4 Ω	–	7.0	–	W
		R_L = 2 Ω	–	13.0	–	W
SVRR	s ly vo age ripple rejection		46	–	–	dB
$V_{n(o)}$	nois outpu voltage	R_S = 0 Ω	–	50	–	µV
$\|Z_i\|$	input impedance		50	–	–	kΩ

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8512J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

6 BLOCK DIAGRAM

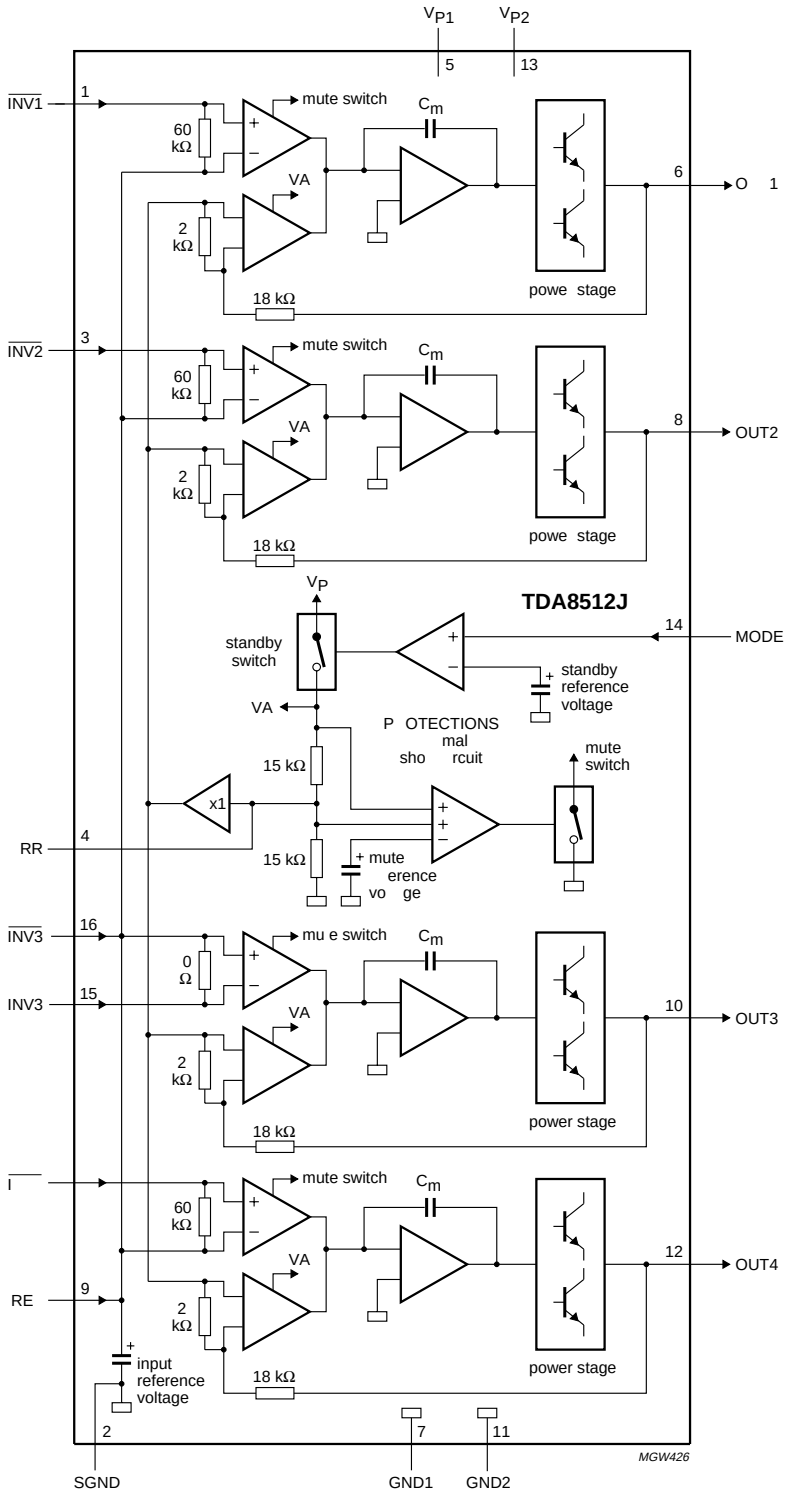


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{INV1}$	1	non-inverting input 1
SGND	2	signal ground
$\overline{INV2}$	3	non-inverting input 2
RR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage 1
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
REF	9	reference voltage input
OUT3	10	output 3
GND2	11	power ground 2
OUT4	12	output 4
V_{P2}	13	supply voltage 2
MODE	14	mode select switch input
INV3	15	inverting input 3
$\overline{INV3}$	16	non-inverting input 3
$\overline{INV4}$	17	non-inverting input 4

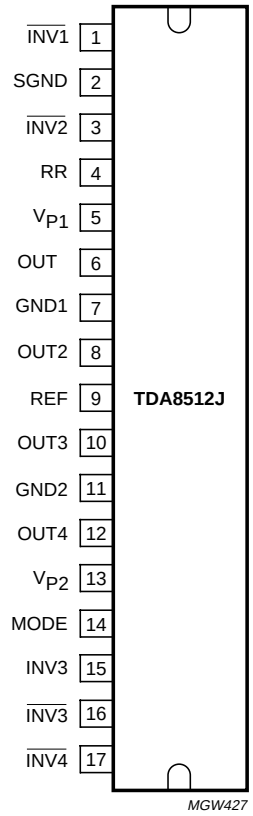


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

The TDA8512J contains four identical amplifiers and can be used in the configurations:

- Two SE channels (fixed gain 20 dB) and one BTL channel (fixed gain 26 dB)
- Four SE channels.

(R_L depends on the application).

8.1 Mode select switch

A special feature of the TDA8512J device is the mode select switch (pin MODE), offering:

- Low standby current (<100 μA)
- Low switching current (low cost supply switch)
- Mute facility.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode for longer than 100 ms to allow charging of the input capacitors at pins $\overline{INV1}$, $\overline{INV2}$, INV3, $\overline{INV3}$ and $\overline{INV4}$. This can be achieved by:

- Control via a microcontroller
- An external timing circuit (see Fig.3).

The circuit slowly ramps up the voltage at the pin MODE when switching on, and results in fast muting when switching off.

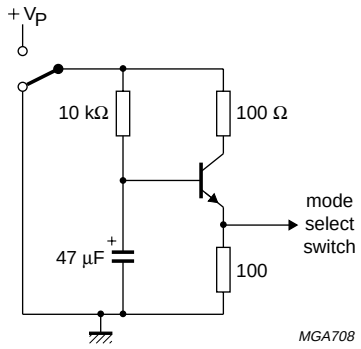


Fig Mode select switch circuitry.

8.2 Mode select

For the 3 functional modes; standby, mute and operate, the pin MODE can be driven by a 3-state logic output stage: e.g. microcontroller with some external components for DC level shifting. (see Fig 10).

Standby mode will be activated by applying a low DC level between 0 and 2 V. The power consumption of the device will be reduced to less than 1.5 mW. The input and output pins are floating high impedance condition.

Mute mode will be activated by a applying a DC level between 3.3 and 6.4 V. The outputs of the amplifier will be muted (no audio output); however, the amplifier is DC biased and the DC level of the input and output pins stays on half the supply voltage.

Operating mode is obtained at a DC level between 8.5 V and V_P

8.3 Built-in protection circuits

The device contains both a thermal protection, and a short-circuit protection.

Thermal protection:

The junction temperature is measured by a temperature sensor; at a junction temperature of about 160 °C this detection circuit switches off the power stages.

Short-circuit protection (outputs to ground, supply and across the load):

Short-circuit is detected by a so called Maximum Current Detection circuit, which measures the current in the positive, respectively negative supply line of each power stage. At currents exceeding (typical) 6 A, the power stages are switched off during some ms.

8.4 Short-circuit protection

When a short-circuit during operation to either GND or across the load of one or more channels occurs, the output stages are switched off for approximately 20 ms. After that time, it is checked during approximately 50 μs to see whether the short-circuit is still present. Due to this duty factor of 50 μs per 20 ms, the average supply current is very low during this short-circuit (approximately 40 mA, see Fig.4).

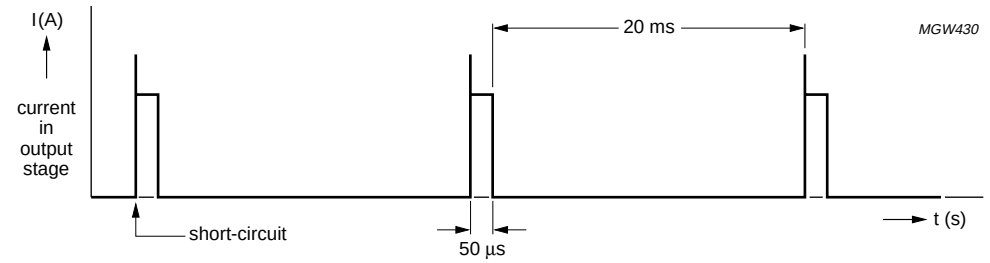


Fig.4 Short-circuit wa e form.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating Sy em (IE 601 4).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	opera ing	–	18	V
		o signal	–	21	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
V_{sc}	short-circuit safe voltage	op rating; note 1	–	18	V
V_{rp}	reverse polarity volta		–	6	V
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperatur		–55	+150	°C
T_{amb}	ambient tempera ure		–40	+85	°C
T_{vj}	virtual junc temperature		–	150	°C

Note

1. To ground and acro s load.

10 HANDLING

ESD protection o his d vice complies with the Philips' General Quality Specification (GQS).

11 THERMAL CHARACTERISTICS

In accordance with IEC 60747-1.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40.0	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	see Fig.5	1.3	K/W

The measured thermal resistance of the IC-package ($R_{th(j-c)}$) is maximum 1.3 K/W if all four channels are driven. For a maximum ambient temperature of 60 °C and V_P = 15 V, the following calculation for the heatsink can be made:

For the application two SE outputs with 2 Ω load, the measured worst-case sine-wave dissipation is 2 × 7 W

For the application BTL output with 4 Ω load, the worst-case sine-wave dissipation is 12.5 W.

So the total power dissipation is $P_{d(tot)} = 2 \times 7 + 12.5$ W = 26.5 W.

At $T_{j(max)}$ = 150 °C the temperature increase, caused by the power dissipation, is: ΔT = 150 °C – 60 °C = 90 °C.

So $P_{d(tot)} \times R_{th(tot)} = \Delta T$ = 90 K. As a result: $R_{th(tot)} = \frac{90}{26.5} = 3.4$ K/W which means:

$R_{th(hs)} = R_{th(tot)} - R_{th(j-c)} = 3.4 - 1.3 = 2.1$ K/W.

The above calculation is for application at worst-case (stereo) sine-wave output signals. In practice, music signals will be applied. In that case the maximum power dissipation will be about three times the sine-wave power dissipation, which allows the use of a smaller heatsink.

So $P_{d(tot)} \times R_{th(tot)} = \Delta T$ = 90 K. As a result: $R_{th(tot)} = \frac{90}{13\frac{1}{5}} = 6.8$ K/W which means:

$R_{th(hs)} = R_{th(tot)} - R_{th(j-c)} = 6.8 - 1.3 = 5.5$ K/W.

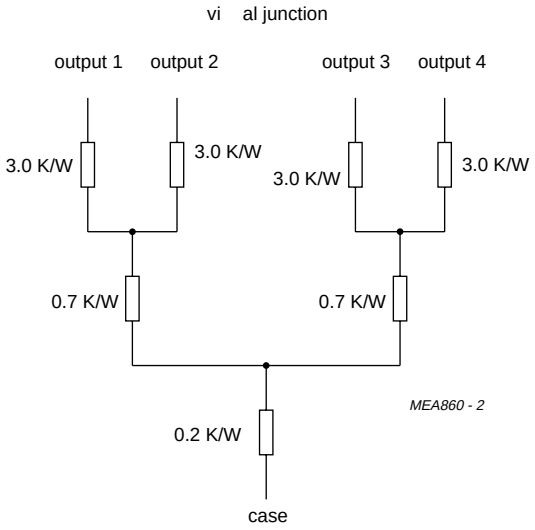


Fig.5 Equivalent thermal resistance network.

12 DC CHARACTERISTICS

V_P = 15 V; T_{amb} = 25 °C; measured according to Figs 6 and 7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6	15	18	V
$I_{q(tot)}$	total quiescent current		–	0	0	mA
V_O	DC output voltage		–	6.9	–	V
$\lvert\Delta V_{OO}\rvert$	DC output offset voltage	note 2	–		150	mV
Mode select switch						
$V_{sw(on)}$	switch-on voltage		5	–	–	V
Mute condition						
V	mute voltage		3.3	–	6.4	V
V_O	output voltage	$V_{i(max)}$ = 1 V; f_i = 1 kH	–	–	2	mV
$\lvert\Delta V_{OO}\rvert$	DC output offset voltage	note 2		–	150	mV
Standby condition						
V_{stb}	standby voltage		0	–	2	V
I_{stb}	standby current		–	–	100	µA
$I_{sw(on)}$	switch-on current		–	12	40	µA

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and C operat ng at V_P = 8.5 to 18 V.
2. Only for BTL channel ($V_{OUT4} - V_{OUT3}$).

13 AC CHARACTERISTICS

V_P = 15 V; f_i = 1 kHz; T_{amb} = 25 °C; bandpa s 22 Hz o 22 kHz; measured according to Figs 6 and 7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BTL channel						
P_o	output power	R_{L2} = 4 Ω (see Fig.7); note 1				
		THD = 0.5%	16	20	–	W
		THD = 10%	22	26	–	W
THD	total harm nic dist t n	P_o = 1 W	–	0.06	–	%
B_P	power bandw dth	THD = 0.5%; P_o = –1 dB with respect to 17 W	–	20 to 15000	–	Hz
$f_{ro(l)}$	low frequ ncy roll-off	at –1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high freq e y roll-off	at –1 dB	20	–	–	kHz
G_V	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	note 3;				
		operating	48	–	–	dB
		mute	46	–	–	dB
		standby	80	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Z_i\|$	input impedance		25	30	38	kΩ
$V_{n(o)}$	noise output voltage	operating; R_s = 0 Ω; note 4	–	70	–	μV
		operating; R_s = 10 kΩ; note 4	–	100	2 0	μV
		mute; notes 4 and 5	–	60	–	μV
SE channels						
P_o	output power	R_{L1} = 2 Ω (see Fig.7); note 1				
		THD = 0.5%	8.0	10	–	W
		THD = 10%	11.	13.0	–	W
		R_{L1} = 4 Ω (see Fig.7); note 1				
		THD = 0.5%	–	5.5	–	W
		THD = 10%	–	7.0	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.06	–	%
$f_{ro(l)}$	low frequency roll-off	at –1 dB; note 2		25	–	Hz
$f_{ro(h)}$	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		19	20	21	dB
SVRR	supply voltage ripple rejection	note 3;				
		operating	48	–	–	dB
		mute	46	–	–	dB
		stan by	80	–	–	dB
$\|Z_i\|$	input impedance		50	60	75	kΩ
$V_{n(o)}$	noise output voltage	op rating R = 0 Ω; note 4	–	50	–	μV
		operat g; R_s = 10 kΩ; note 4	–	70	100	μV
		mute; notes 4 and 5	–	50	–	μV
α_{cs}	channel separation	R_s = 1 kΩ	40	60	–	dB
$\|\Delta G_V\|$	channel unbalance		–	–	1	dB

Notes

1. Output power is measured di ectly a he output pins of the device.
2. Frequency response externally xed.
3. Ripple rejection measured at e o tput with a source impedance of 0 Ω; maximum ripple of 2 V (p-p) and at a frequency between 100 Hz t 10 kHz.
4. Noise measured in bandw dt of 20 Hz to 20 kHz.
5. Noise output voltage independant of R_s (V_i = 0 V).

14 APPLICATION INFORMATION

14.1 Input configuration

- Inputs 1 and 2 are used for SE application on pin OUT1, respectively pin OUT2
- Input 3 can be configured for both SE and BTL application
- Input 4 can be used for SE application of pin OUT4, or for BTL application together with input 3. See Figs 6 and 7.

Note that the DC level of all input pins is half the supply voltage V_P, so coupling capacitors for the input pins are necessary!

Cut-off frequency for the input is: $f_{i(co)}$ = 12 Hz. Therefore it is not necessary to use high capacitor values on the input; so the delay during switch-on, which is necessary for charging the input capacitors, can be minimised. This results in a good low frequency response and good switch-on behaviour.

14.2 Output power

The output power versus supply voltage has been measured on the output pins of one channel, and at THD = 10%. The maximum output power is limited b the maximum supply voltage of 18 V and the ma imum available output current: 4 A repetitive peak curr nt.

14.3 Power dissipation

The power dissipation graphs are given for ne output channel in SE, respectively BTL application. So for total worst-case power dissipation the P_d of each ha nel must be added up.

14.4 Supply Voltage Ripple Re ection (SVRR)

The SVRR is measured with electr lytic capacitor of 100 µF on pin RR and at a ban width 10 Hz to 80 kHz, whereas the lowest frequ ies c n be lower than 10 Hz.

Proper supply bypassing s critical for low noise performance and hi h pow r supply rejection. The respective capacitor ocati should be as close to the device as possible and grounded to the power ground. A proper power supply d co pling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR (typical 0.1 µF) has to be placed as close as possible to the device. For suppressing lower frequency noise a d ripple signals, a large electrolytic capacitor (e.g.1000 µF o more) must be placed close to the device

The bypass capacitor on the n RR du es the noise and ripple on the mid rail voltage. F good THD and noise performance, a low ESR capacitor recommended.

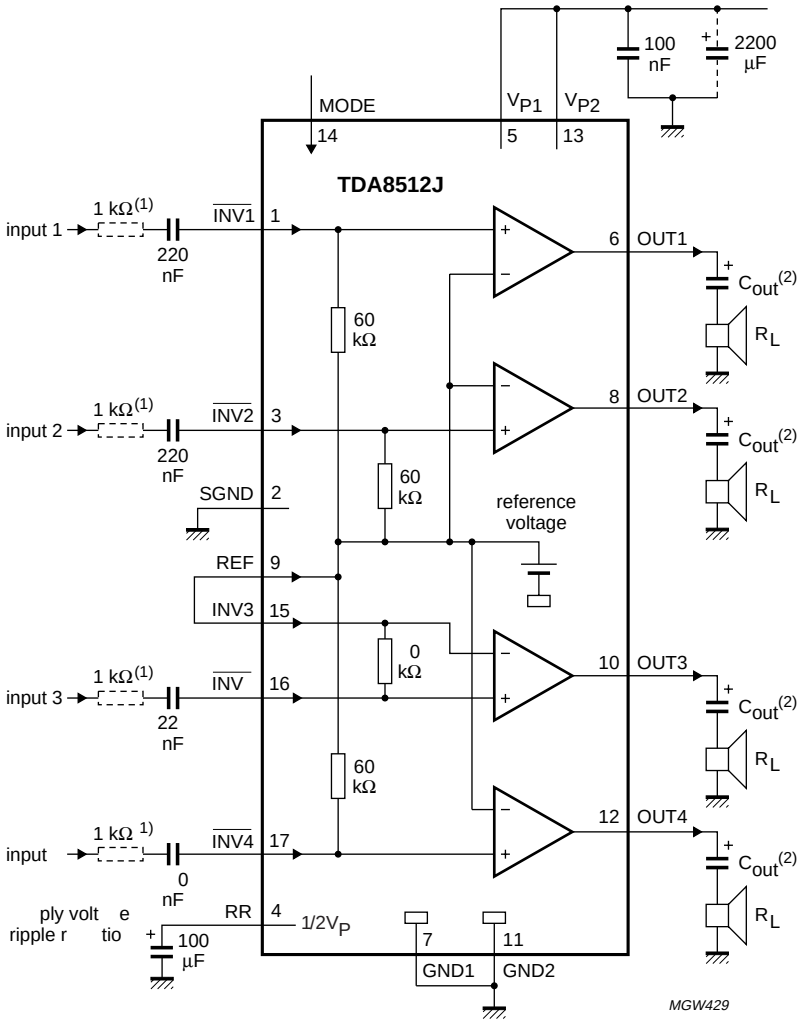
14.5 Switch-on and switch-of

To avoid audible plops du g switching on and switching off the supply voltage he pin MODE has to be set in standby condition (<2V) b fore the voltage is applied (switch-on) or removed (switch-off). Via the mute mode, the input- a d SVRR-capacitors are smoothly charged.

The turn on a d turn-off time can be influenced by an RC-c cuit on t e pin MODE (see Fig.3). Rapidly switching on and ff of the device or the pin MODE, may cause “click a pop” oise. This can be prevented by a proper timing on e pin MODE.

14.6 CB layout and grounding

r high system performance level certain grounding techniques are imperative. The input reference grounds have to be tied with their respective source grounds, and must have separate traces from the power ground traces; this will separate the large (output) signal currents from interfering with the small AC input signals. The small-signal ground traces should be physically located as far as possible from the power ground traces. Supply- and output-traces should be as wide as practical for delivering maximum output power. The PCB layout, which accommodates the TDA8510, TDA8511, and TDA8512 products, is shown in Fig.8.



(1) Advised when driven with hard clipping input signals.

(2) For frequencies down to 20 Hz:
C_{out} = 4700 µF at R_L = 2 Ω.
C_{out} = 2200 µF at R_L = 4 Ω.

Fig.6 Application diagram for four SE amplifiers.