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Preface

This reference manual describes in detail the hardware on the 56F805 Evaluation Module.

Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F805 part.

Organization

This manual is organized into two chapters and two appendixes.

- **Chapter 1, Introduction -** provides an overview of the EVM and its features.
- **Chapter 2, Technical Summary -** describes in detail the 56F805EVM hardware.
- **Appendix A, 56F805EVM Schematics -** contains the schematics of the 56F805EVM.
- **Appendix B, 56F805EVM Bill of Material -** provides a list of the materials used on the 56F805EVM board.

Suggested Reading

Documentation on the 56F805 and the 56F805EVM kit may be found at this URL:

http://www.freescale.com

Notation Conventions

This document uses the following conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	$\overline{WE}$ $\overline{OE}$	In schematic drawings, Active Low Signals may be noted by a backslash: /WE
Hexadecimal Values	Begin with a “$” symbol	$0FF0 $80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter “b” attached to the number	b1010 b0011	
Numbers	Considered positive unless specifically noted as a negative value	5 -10	Voltage is often shown as positive: +3.3V
Bold	Reference sources, paths, emphasis	...see: **http://www.freescale.com**	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

A/D	Analog-to-Digital
CAN	Controller Area Network, a serial communications peripheral and method
CiA	CAN in Automation, an international CAN user's group that coordinates standards for CAN communications protocols
D/A	Digital-to-Analog
EVM	Evaluation Module
GPIO	General Purpose Input and Output Port
IC	Integrated Circuit
JTAG	Joint Test Action Group, a bus protocol/interface used for test and debug
LQFP	Low-profile Quad Flat Pack
MPIO	Multi Purpose Input and Output Port; shares package pins with other peripherals on the chip and can function as a GPIO
OnCE™	On-Chip Emulation, a debug bus and port created by Freescale to enable designers to create a low-cost hardware interface for a professional-quality debug environment
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface Port
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter

References

The following sources were referenced to produce this manual:

[1] *DSP56800 Family Manual*, Freescale Semiconductor, DSP56800FM

[2] *DSP56F801/803/805/807 User's Manual*, Freescale Semiconductor, DSP56F801-7UM

[3] *56F805 Technical Data*, Freescale Semiconductor, DSP56F805

[4] *CiA Draft Recommendation DR-303-1, Cabling and Connector Pin Assignment*, Version 1.0, CAN in Automation

[5] *CAN Specification 2.0B*, BOSCH or CAN in Automation

Chapter 1
Introduction

The 56F805EVM is used to demonstrate the abilities of the 56F805 and to provide a hardware tool allowing the development of applications that use the 56F805.

The 56F805EVM is an evaluation module board that includes a 56F805 part, peripheral expansion connectors, external memory and a CAN interface. The expansion connectors are for signal monitoring and user feature expandability.

The 56F805EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800 architecture. The tools and examples provided with the 56F805EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/OnCE™ port. The breakpoint features of the OnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full-speed, until the break conditions are satisfied. The ability to examine and modify all user accessible registers, memory and peripherals through the OnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the controller's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the chip are available to the user.

1.1 56F805EVM Architecture

The 56F805EVM facilitates the evaluation of various features present in the 56F805 part. The 56F805EVM can be used to develop real-time software and hardware products based on the 56F805. The 56F805EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the customer's application-specific device(s). The 56F805EVM is flexible enough to allow a user to fully exploit the 56F805's features to optimize the performance of his product, as shown in **Figure 1-1**.

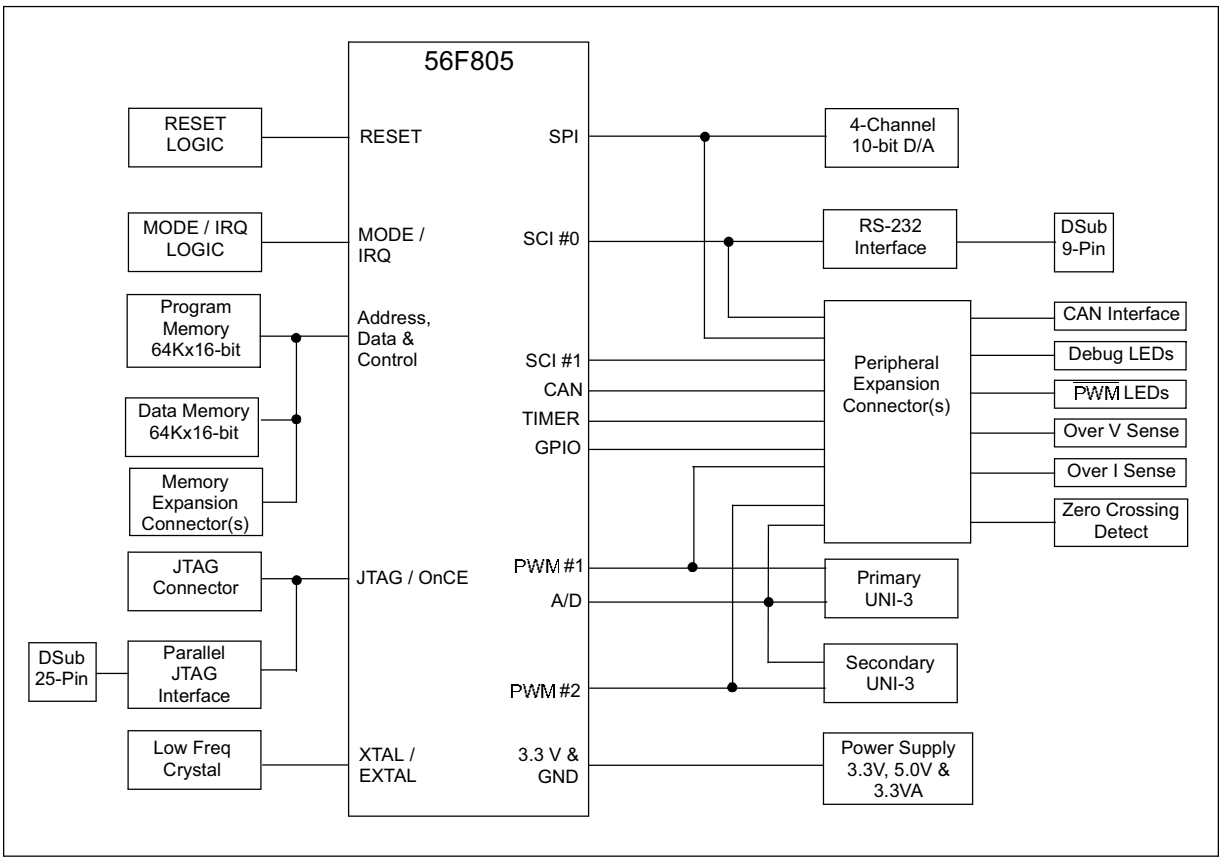

Figure 1-1. Block Diagram of the 56F805EVM

1.2 56F805EVM Configuration Jumpers

Eighteen jumper groups, (JG1-JG18), shown in **Figure 1-2**, are used to configure various features on the 56F805EVM board. **Table 1-1** describes the default jumper group settings.

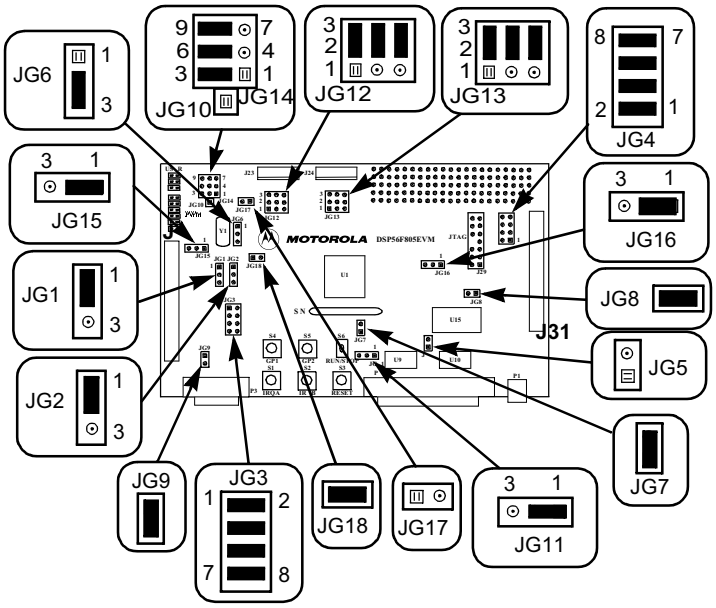

Figure 1-2. 56F805EVM Jumper Reference

Table 1-1. 56F805EVM Default Jumper Options

Jumper Group	Comment	Jumpers Connections
JG1	PD0 input selected as a high	1–2
JG2	PD1 input selected as a high	1–2
JG3	Primary UNI-3 serial selected	1–2, 3–4, 5–6 & 7–8
JG4	Secondary UNI-3 serial selected	1–2, 3–4, 5–6 & 7–8
JG5	Enable on-board Parallel JTAG Host Target Interface	NC
JG6	Use on-board crystal for oscillator input	2–3
JG7	Selects the device's Mode 0 operation upon exit from reset	1-2
JG8	Enable on-board SRAM	1–2
JG9	Enable RS-232 output	1–2

Table 1-1. 56F805EVM Default Jumper Options (Continued)

Jumper Group	Comment	Jumpers Connections
JG10	Secondary UNI-3 Analog Temperature Input unused	1–2
JG11	Use Host power for Host Target Interface	1–2
JG12	Primary Encoder Input Selected	2–3, 5–6 & 8–9
JG13	Secondary Encoder Input Selected	2–3, 5–6 & 8–9
JG14	Primary UNI-3 3-Phase Current Sense Selected as Analog Inputs	2–3, 5–6 & 8–9
JG15	Primary UNI-3 Phase A Over-Current Selected for FAULTA1	1–2
JG16	Secondary UNI-3 Phase B Over-Current Selected for FAULTB1	1–2
JG17	CAN termination unselected	NC
JG18	Use on-board crystal for oscillator input	1–2

1.3 56F805EVM Connections

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and the external +12V DC power supply to the 56F805EVM board.

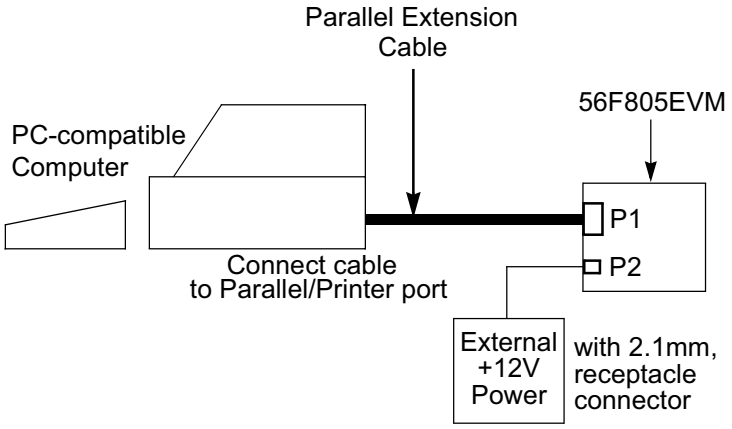

Figure 1-3. Connecting the 56F805EVM Cables

Perform the following steps to connect the 56F805EVM cables:

1. Connect the parallel extension cable to the Parallel port of the host computer
2. Connect the other end of the parallel extension cable to P1, shown in **Figure 1-3**, on the 56F805EVM board. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12V DC, 4.0A power supply is not plugged into a 120V AC power source
4. Connect the 2.1mm output power plug from the external power supply into P2, shown in **Figure 1-3**, on the 56F805EVM board
5. Apply power to the external power supply. The green Power-On LED, LED10, will illuminate when power is correctly applied.

Chapter 2
Technical Summary

The 56F805EVM is designed as a versatile controller development card for developing real-time software and hardware products to support a new generation of applications in digital and wireless messaging, servo and motor control, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F805 controller, combined with the on-board 64K × 16-bit external program static RAM (SRAM), 64K × 16-bit external data SRAM, CAN interface, Hall-Effect/Quadrature Encoder interface, motor zero crossing logic, motor bus over-current logic, motor bus over-voltage logic and parallel JTAG interface, makes the 56F805EVM ideal for developing and implementing many motor controlling algorithms, as well as for learning the architecture and instruction set of the 56F805 processor.

The main features of the 56F805EVM include:

- 56F805 16-bit +3.3V controller operating at 80MHz [U1]
- External fast static RAM (FSRAM) memory [U15], configured as:
  - 64K×16 bits of program memory with 0 wait states at 70MHz
  - 64K×16 bits of data memory with 0 wait states at 70MHz
- 4-Channel 10-bit Serial D/A, SPI for real-time user data display [U18]
- 8.00MHz crystal oscillator for frequency generation [Y1]
- Optional external oscillator frequency input connector [JG6 and JG18]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J29]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P1]
- RS-232 interface for easy connection to a host processor [U16 and P3]
- CAN interface for high speed, 1.0Mbps, communications [U20 and J26]
- CAN bypass and bus termination [J32 and JG17]
- Connector to allow the user to connect his own SPI0 / MPIO-compatible peripheral [J16]

- Connector to allow the user to connect his own SCI1 / MPIO-compatible peripheral [J17]
- Connector to allow the user to connect his own SPI / MPIO-compatible peripheral [J19]
- Connector to allow the user to connect his own PWMA or MPIO-compatible peripheral [J21]
- Connector to allow the user to connect his own PWMB / MPIO-compatible peripheral [J22]
- Connector to allow the user to connect his own CAN physical layer peripheral [J25]
- Connector to allow the user to connect his own Timer A / MPIO-compatible peripheral [J3]
- Connector to allow the user to connect his own Timer B / MPIO-compatible peripheral [J6]
- Connector to allow the user to connect his own Timer C / MPIO-compatible peripheral [J8]
- Connector to allow the user to connect his own Timer D / MPIO-compatible peripheral [J5]
- Connector to allow the user to attach his own Port B GPIO-compatible peripheral [J28]
- Connector to allow the user to attach his own Port D GPIO-compatible peripheral [J4]
- Connector to allow the user to attach his own Port E GPIO-compatible peripheral [J7]
- 56F805's external memory expansion connectors [J1, J2 and J27]
- On-board power regulation from an external +12V DC-supplied power input [P2]
- Light Emitting Diode (LED) power indicator [LED10]
- Three on-board real-time user debugging LEDs [LED1-3]
- Six on-board Primary PWM monitoring LEDs [LED4-9]
- Primary UNI-3 Motor interface [J30]

  Encoder/Hall-Effect interface

  Over-Voltage sensing [U8]

  Over-Current sensing [U5]

  Phase Current sensing [U8 and U21]

  Back-EMF sensing

  Temperature sensing

  Zero Crossing detection

  Pulse Width Modulation