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1 General description

The GD32F190xx device belongs to the 5V value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance ARM® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F190xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 72 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to five general-purpose 16-bit timers, a general-purpose 32-bit timer, a basic timer, a PWM advanced-control timer, as well as standard and advanced communication interfaces: up to three SPIs, three I^2Cs and two USARTs, two I^2S, two CAN2.0B with a CAN PHY, and a segment LCD controller. Advanced analog peripherals including one 12-bit ADC, two 12-bit DACs, three OP-AMPs and two comparators.

The device operates from a 2.5 to 5.5V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F190xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, home appliances, E-bike and so on.

2 Device overview

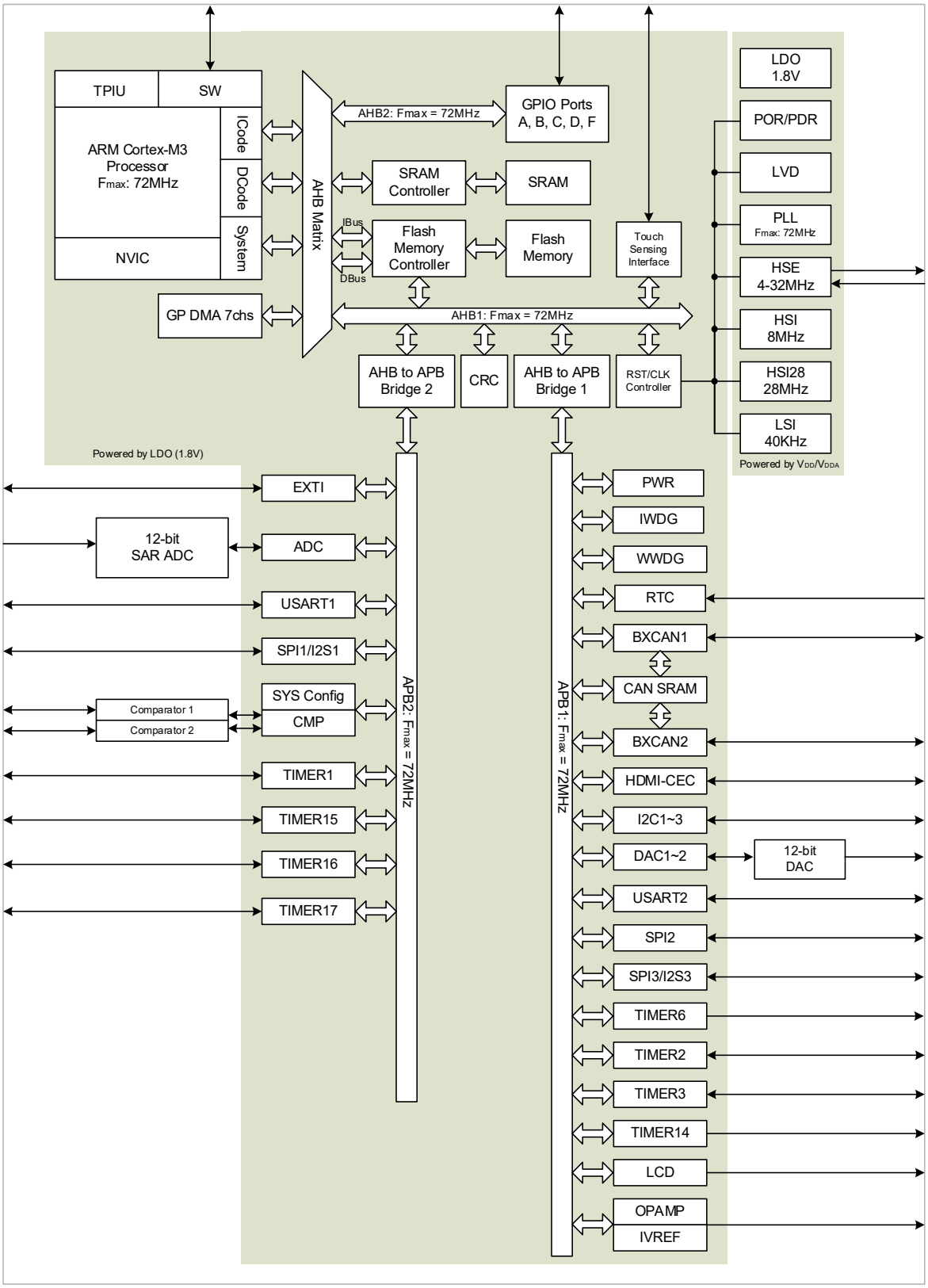
2.1 Device information

Table 1. GD32F190xx devices features and peripheral list

Part Number		GD32F190xx								
		T4	T6	T8	C4	C6	C8	R4	R6	R8
Flash (KB)		16	32	64	16	32	64	16	32	64
SRAM (KB)		4	6	8	4	6	8	4	6	8
Timers	32-bit GP	1	1	1	1	1	1	1	1	1
	16-bit GP	5	5	5	5	5	5	5	5	5
	16-bit Adv.	1	1	1	1	1	1	1	1	1
	16-bit Basic	1	1	1	1	1	1	1	1	1
	SysTick	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1
Connectivity	USART	1	2	2	1	2	2	1	2	2
	I2C	1	1	3	1	1	3	1	1	3
	SPI	1	1	3	1	1	3	1	1	3
	I2S	1	1	2	1	1	2	1	1	2
	CAN 2.0B	2	2	2	2	2	2	2	2	2
	LCD	0	0	0	4x18	4x18	4x18	8x32	8x32	8x32
GPIO		28	28	28	39	39	39	55	55	55
Capacitive Touch Channels		14	14	14	17	17	17	18	18	18
OP-AMP		2	2	2	2	2	2	3	3	3
Analog Comparator		2	2	2	2	2	2	2	2	2
EXTI		16	16	16	16	16	16	16	16	16
ADC	Units	1	1	1	1	1	1	1	1	1
	Channels (Ext.)	10	10	10	10	10	10	16	16	16
	Channels (Int.)	3	3	3	3	3	3	3	3	3
DAC		2	2	2	2	2	2	2	2	2
Package		QFN36			LQFP48			LQFP64		

2.2 Block diagram

Figure 1. GD32F190xx block diagram



2.3 Pinouts and pin assignment

Figure 2. GD32F190Rx LQFP64 pinouts

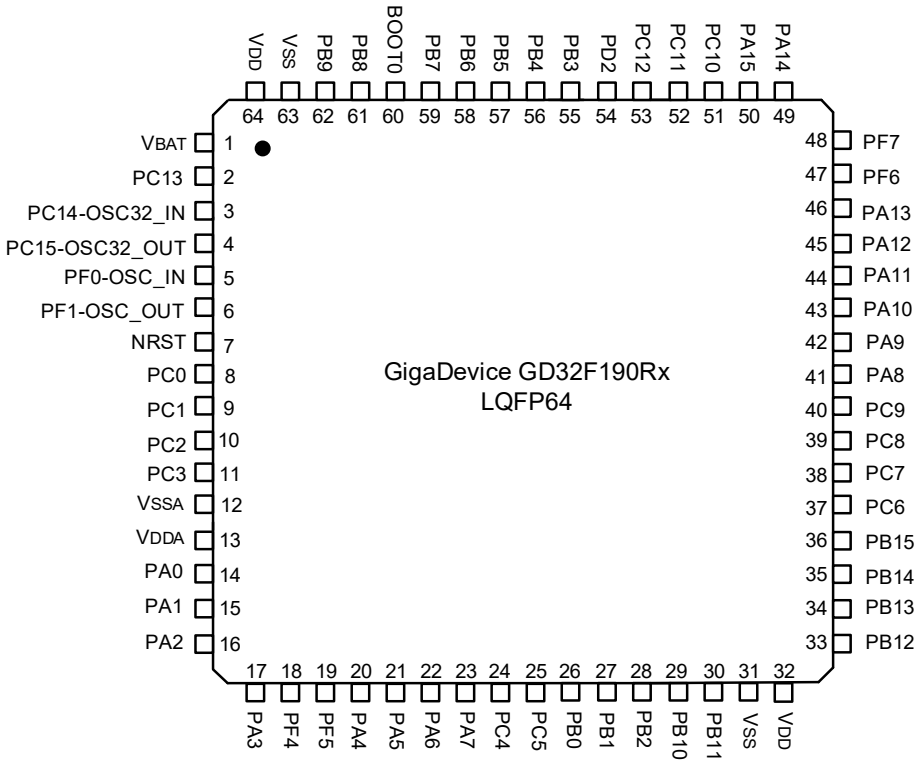


Figure 3. GD32F190Cx LQFP48 pinouts

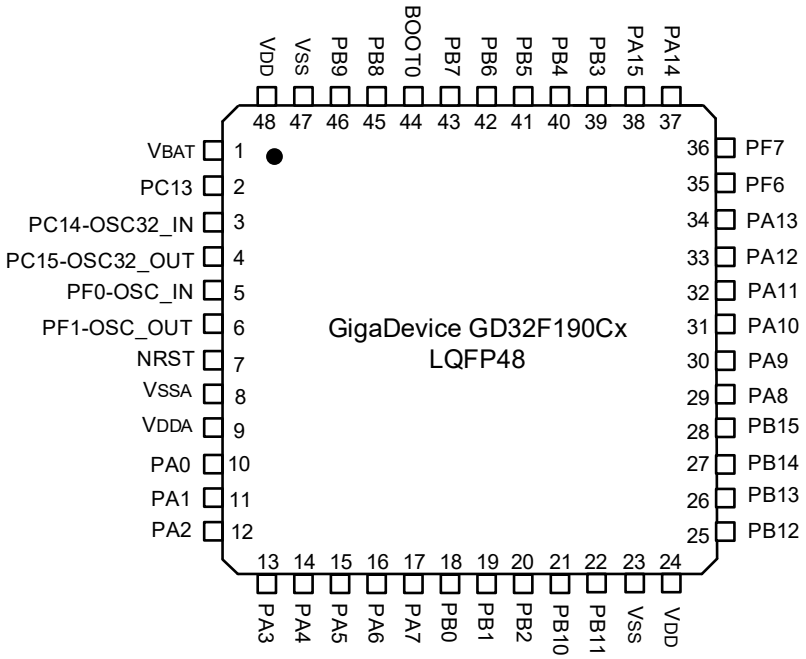
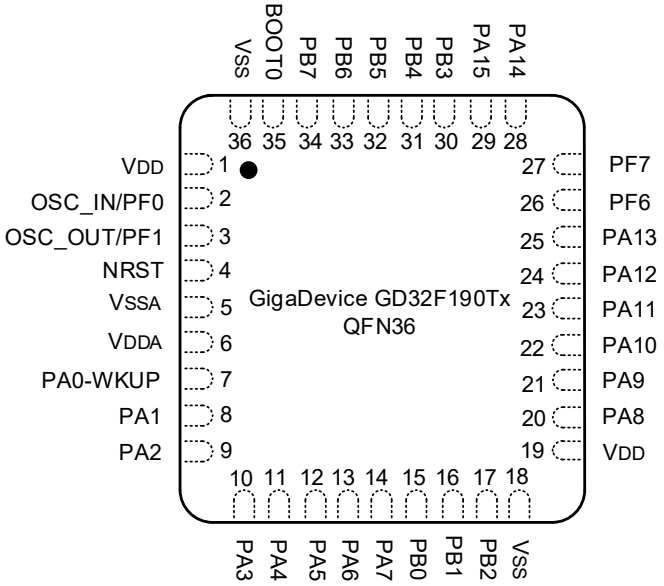
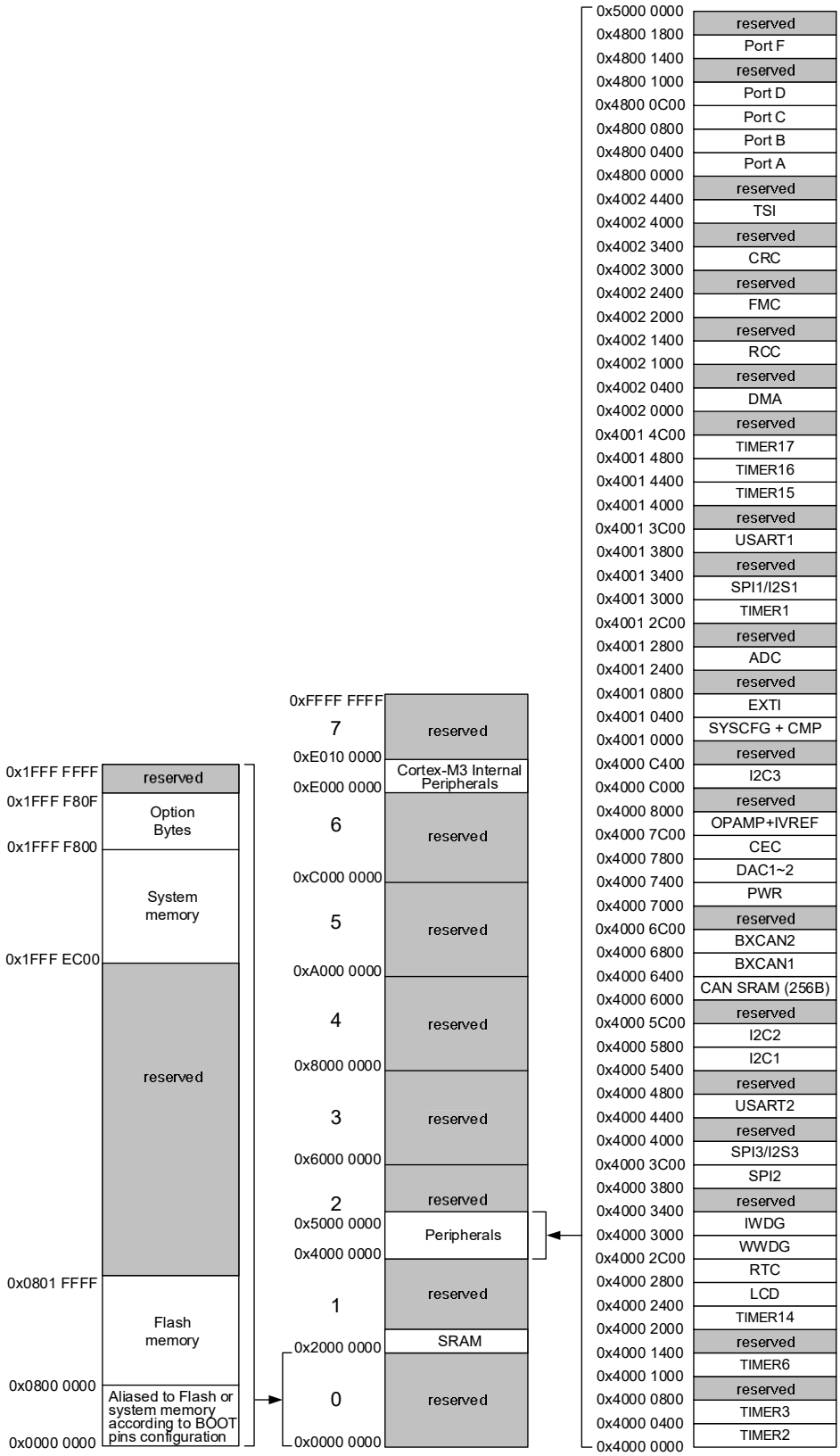


Figure 4. GD32F190Tx QFN36 pinouts



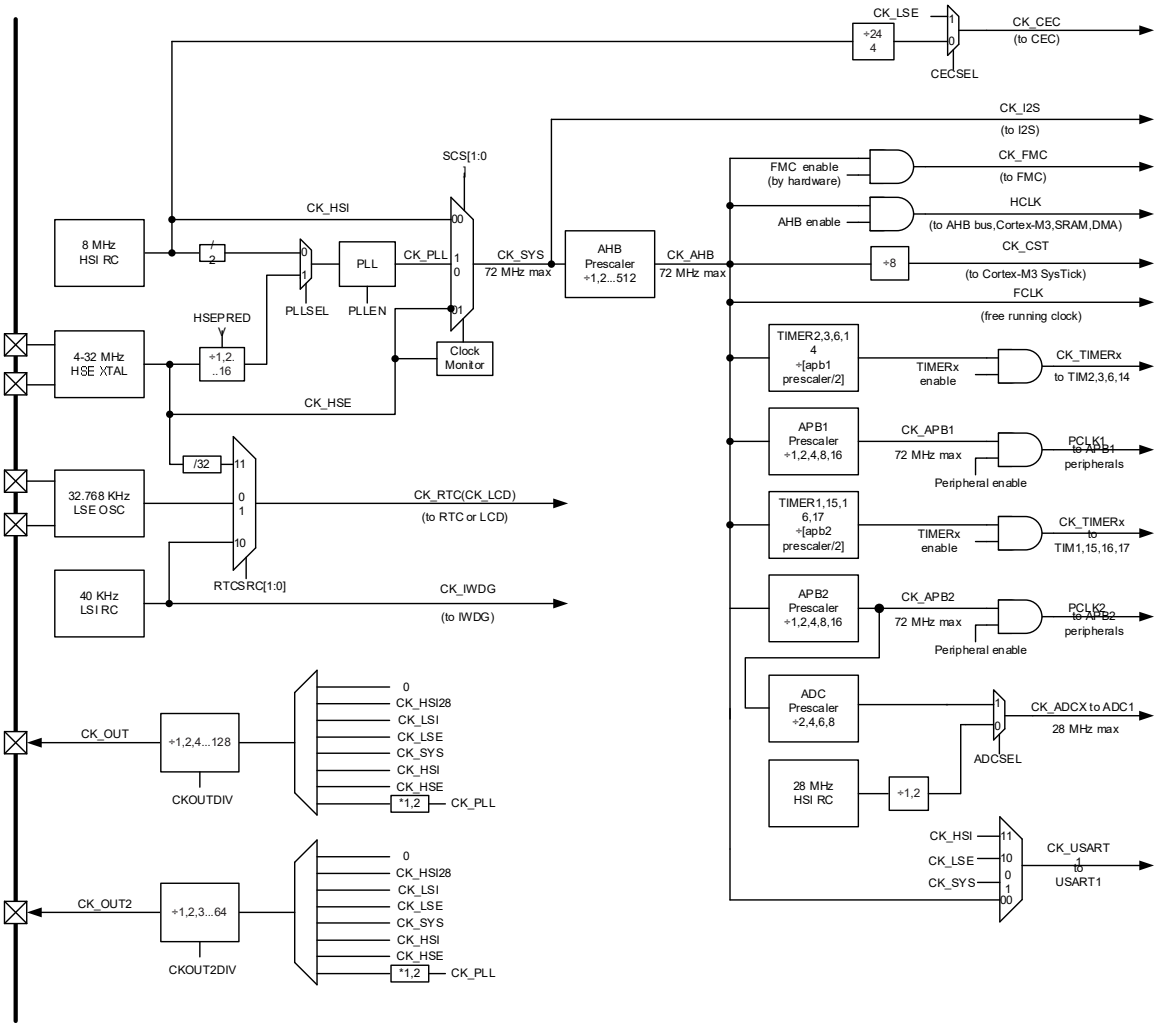
2.4 Memory map

Figure 5. GD32F190xx memory map



2.5 Clock tree

Figure 6. GD32F190xx clock tree



Legend:

HSE = High speed external clock

HSI = High speed internal clock

LSE = Low speed external clock

LSI = Low speed internal clock

2.6 Pin definitions

Table 2. GD32F190xx pin definitions

Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN36			
V_{LCD}/V_{BAT}	1	1	-	P		Default: V_{LCD}/V_{BAT}
PC13-TAMPER-RTC	2	2	-	I/O		Default: PC13 Additional: RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
PC14-OSC32_IN	3	3	-	I/O		Default: PC14 Additional: OSC32_IN
PC15-OSC32_OUT	4	4	-	I/O		Default: PC15 Additional: OSC32_OUT
PF0-OSC_IN	5	5	2	I/O	HVT	Default: PF0 Additional: OSC_IN
PF1-OSC_OUT	6	6	3	I/O	HVT	Default: PF1 Additional: OSC_OUT
NRST	7	7	4	I/O		Default: NRST
PC0	8	-	-	I/O		Default: PC0 Alternate: EVENTOUT, I2C3_SCL, SEG18 Additional: ADC_IN10
PC1	9	-	-	I/O		Default: PC1 Alternate: EVENTOUT, I2C3_SDA, SEG19 Additional: ADC_IN11, OPAMP3_VINP
PC2	10	-	-	I/O		Default: PC2 Alternate: EVENTOUT, I2C3_SMBA, SEG20 Additional: ADC_IN12, OPAMP3_VINM
PC3	11	-	-	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC_IN13, OPAMP3_VOUT, SEG21, I2C3_TXFRAME
V_{SSA}	12	8	5	P		Default: V_{SSA}
V_{DDA}	13	9	6	P		Default: V_{DDA}
PA0-WKUP	14	10	7	I/O		Default: PA0 Alternate: USART1_CTS(3), USART2_CTS(4), TM2_CH1_ETR, I2C2_SCL, CMP1_OUT, TSI_G1_IO1 Additional: ADC_IN0, RTC_TAMP2, WKUP1, CMP1_INM6
PA1	15	11	8	I/O		Default: PA1 Alternate: USART1_RTS(3), USART2_RTS(4), TM2_CH2, I2C2_SDA, EVENTOUT, SEG0, TSI_G1_IO2 Additional: ADC_IN1, CMP1_INP, OPAMP1_VINP
PA2	16	12	9	I/O		Default: PA2 Alternate: USART1_TX(3), USART2_TX(4), TM2_CH3, TM15_CH1, SEG1, CMP2_OUT, TSC_G1_IO3, I2C2_SMBA