Altera PHYLite for Parallel Interfaces Loopback Reference Designs Application Note

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This application note showcases loopback reference designs using the Altera PHYLite IP core.

This document is divided into three main segments:

- 1. A simple input/output PHYLite simulation reference design.
- **2.** A simple input/output PHYLite with dynamic reconfiguration using Arria 10 devices hardware reference design.
- 3. Functional description for the modules and application used in both reference designs.

Simple Input/Output PHYLite Simulation Design Example

This section provides architecture description and user guide for the simulation reference design.

Simulation Design Example Architecture

The simulation reference design is a simple design that simulates the behavior of the Altera PHYLite IP core. This design consists of 2 main components:

- A device Under Test (DUT) module that includes two Altera PHYLite IP instances.
- A traffic generator module

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Figure 1: Simulation Reference Design Block Diagram



Simulation Reference Design User Guide

Follow these steps to setup and run the simulation reference design.

Requirements

The following are the requirements to run the simulation reference design:

- Quartus Prime Design Suite[®] versions 15.1
- Simulation design example phylite_top_sim_only.par

Related Information

- AN 747 Altera PHYLite Simulation Reference Design Files
- Getting Started with the Design Store Guideline to download and install design examples from Design Store.



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Setting Up Simulation Environment

- 1. Follow the guidelines in Getting Started with the Design Store to download and install the reference design files.
- 2. Open the reference design .qpf file after successfully installing the design templates.
- 3. Click on Assignments -> Settings....
- 4. Select EDA Tools Settings -> Simulation.
- 5. At the Settings window, choose Modelsim-Altera for Tool Name. You may choose VHDL, Verilog HDL or System Verilog as the output netlist format.

Figure 2: Simulation Settings using EDA Tools in the Quartus Prime Software

General	Simulation
Files	Specify options for generating output files for use with other EDA tools.
	Tool name: ModelSim-Altera
 Design Templates Operating Settings and Condition 	Run gate-level simulation automatically after compilation
Voltage Temperature	EDA Netlist Writer settings
Compilation Process Settings	Format for output netlist: Verilog HDL Time scale: 1 ps
EDA Tool Settings	Output directory: simulation/modelsim
Design Entry/Synthesis Simulation	□ Map illegal HDL characters □ □ Enable glitch filtering
Formal Verification Board-Level	Options for Power Estimation
Compiler Settings	Generate Value Change Dump (VCD) file script Script Settings
- Verilog HDL Input - Default Parameters	Design instance name:
TimeQuest Timing Analyzer Assembler	More EDA Netlist Writer Settings
SignalTap II Logic Analyzer	NativeLink settings
Logic Analyzer Interface	C None
SSN Analyzer	Compile test bench: tb
	C Script to compile test bench: simulation/modelsim/runme.do
	More NativeLink Settings
<u>і — і </u>	OK Cancel Apply Help

6. Open dut_INPUT.qsys file and make sure the IP has the same configuration shown below:

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Figure 3: Configuration for dut_INPUT Module

ystem: dut_INPUT Path: phylite_0		System: dut_INPUT Path: phylite_0		
Altera PHYLite for Parallel Interfaces	Details Generate Example Design	Altera PHYLite for Parallel Interfaces		<u>D</u> etails
itera_phylite				Generate Example Design.
Parameters		* Parameters		
Number of groups: 1		Number of groups: 1		
General Group 0		General Group 0		
T Clarks		Crown & Parameter Settings		
Interface clock frequency 800.0 MHz				
Use core PLL reference clock connection		Coby parameters from another group		
Use recommended BL reference clock formulate		Group 0 Pin Settings		
Ose recommended FEC reference clock frequency		Pin type:	Input 💌	
VCO clock frequency: 200.0 MHz		Pin width:	4	
Clock rate of user logic: Quarter		DDR/SDR:	DDR 👻	
Quarter		Group 0 Input Path Settings		
Specify additional output clocks based on existing PLL		Read latency.	9 external	interface clock cycles
* Dynamic Reconfiguration		Swap capture strobe polarity		
Use dynamic reconfiguration		Capture strobe phase shift:	0 degrees	
Interface ID: 0			degrees	
* I/O Settings		" Group 0 Output Path Settings		
I/O standard: SSTI -15 Class I		write latency.	0lexternal	Interface clock cycles
		Use output strobe		
		Output strobe phase:	90 💌 degrees	
		* Group 0 General Data Settings		
		Data configuration:	Single ended 👻	
		* Group 0 General Strobe Settings		
		Strobe configuration:	Single ended	
		Use separate strobes		
		* Group 0 OCT Settings		
		OCT enable size:	1	
		☑ Use Default OCT Values		
		Input OCT Value:	No termination	
		Output OCT Value:	No termination	
		* Group 0 Timing Settings		
		Generate Input Delay Constraints for this group		
		Input Strobe Setup Delay Constraint:	0.03 ns	
		Input Strobe Hold Delay Constraint:	0.03 ns	
		Inter Symbol Interference of the Read Channel	0.09	

- 7. Make sure that the **Capture strobe phase shift** is set to **0** degrees to align the incoming data to strobe edge during data transfer.
- 8. Click Generate HDL... and select your desired simulation model format. Next, click Generate to generate the simulation model for the dut_INPUT module. Click Close and Finish when the generation is complete.

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Figure 4: Generating Simulation Model

Generation <@pg-slscf07>		
▼ Synthesis		
Synthesis files are used to compile th	he system in a Quartus Prime project.	
Create HDL design files for synthesis	5: Verilog 🖵	
Create timing and resource estin	nates for third-party EDA synthesis tools.	
Create block symbol file (.bsf)		
 Simulation 		
The simulation model contains gene	rated HDL files for the simulator, and may include simulation-only features.	
Simulation scripts for this componen	t will be generated in a vendor-specific sub-directory in the specified output directory.	
Follow the guidance in the generated ip-setup-simulation and ip-make-s design.	d simulation scripts about how to structure your design's simulation scripts and how to use the imscript command-line utilities to compile all of the files needed for simulating all of the IP in your	ž
Create simulation model:	Verilog 💌	
Allow mixed-language simulation		
Enable this if your simulator support	s mixed-language simulation.	
Output Directory		
Path:	E/phylite_an/devplatforms/15.1.0/phylite_top_sim_only/phylite_top_sim_only_restored/dut_INP	UT
The path of the generation output d	irectory is fixed relative to the .qsys file.	
Clear output directories for selec	ted generation targets.	
	사실 전에 가지 않는 것 같은 것 있다. 이렇게 있는 것 같은 것 같	
	Generate	ancel

9. From the Quartus[®] Prime software, open dut_OUTPUT.qsys file and make sure the IP has the same configuration shown below:

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