

# Altera PHYLite for Parallel Interfaces Loopback Reference Designs Application Note

2016.01.19

AN-747



Subscribe



Send Feedback

This application note showcases loopback reference designs using the Altera PHYLite IP core.

This document is divided into three main segments:

1. A simple input/output PHYLite simulation reference design.
2. A simple input/output PHYLite with dynamic reconfiguration using Arria 10 devices hardware reference design.
3. Functional description for the modules and application used in both reference designs.

## Simple Input/Output PHYLite Simulation Design Example

This section provides architecture description and user guide for the simulation reference design.

### Simulation Design Example Architecture

The simulation reference design is a simple design that simulates the behavior of the Altera PHYLite IP core. This design consists of 2 main components:

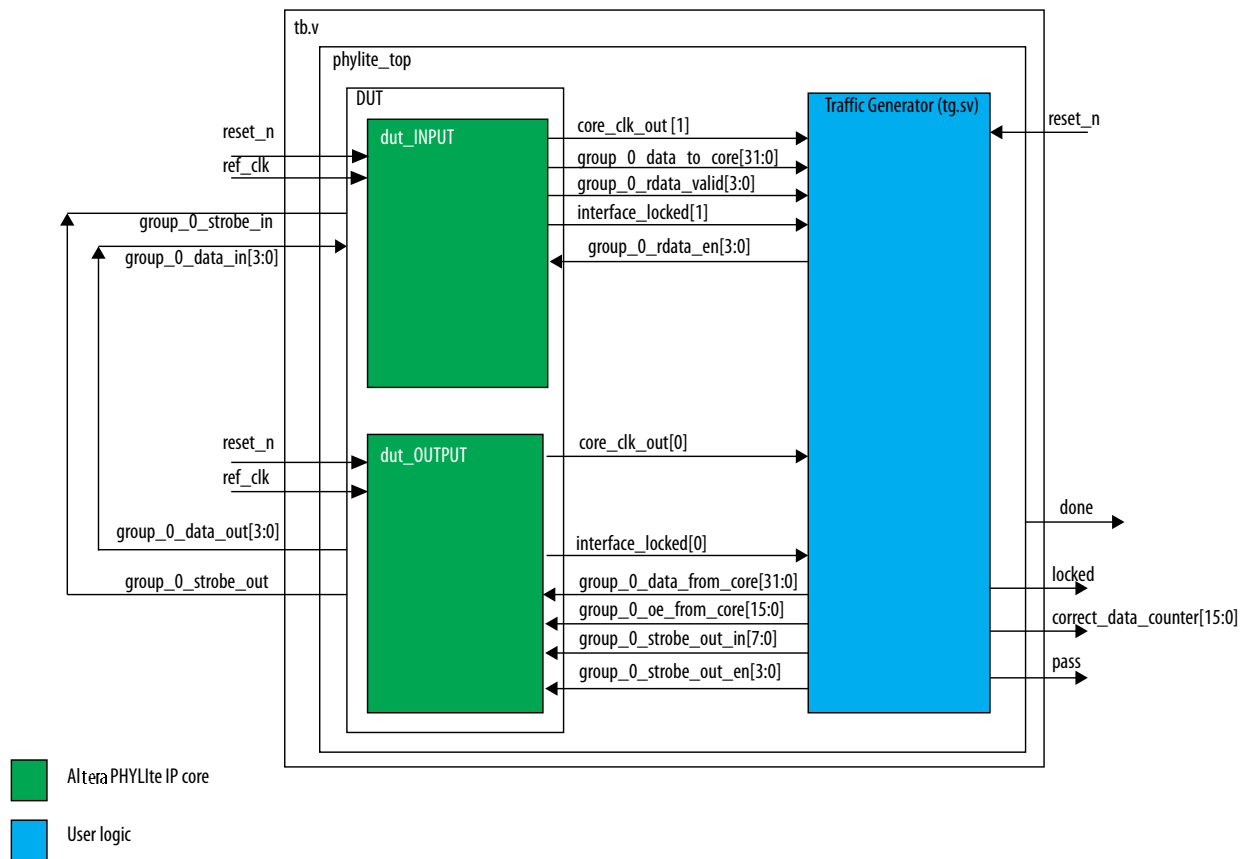
- A device Under Test (DUT) module that includes two Altera PHYLite IP instances.
- A traffic generator module

© 2016 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, ENPIRION, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at [www.altera.com/common/legal.html](http://www.altera.com/common/legal.html). Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

ISO  
9001:2008  
Registered

**ALTERA**  
now part of Intel

Figure 1: Simulation Reference Design Block Diagram



## Simulation Reference Design User Guide

Follow these steps to setup and run the simulation reference design.

### Requirements

The following are the requirements to run the simulation reference design:

- Quartus Prime Design Suite® versions 15.1
- Simulation design example phylite\_top\_sim\_only.par

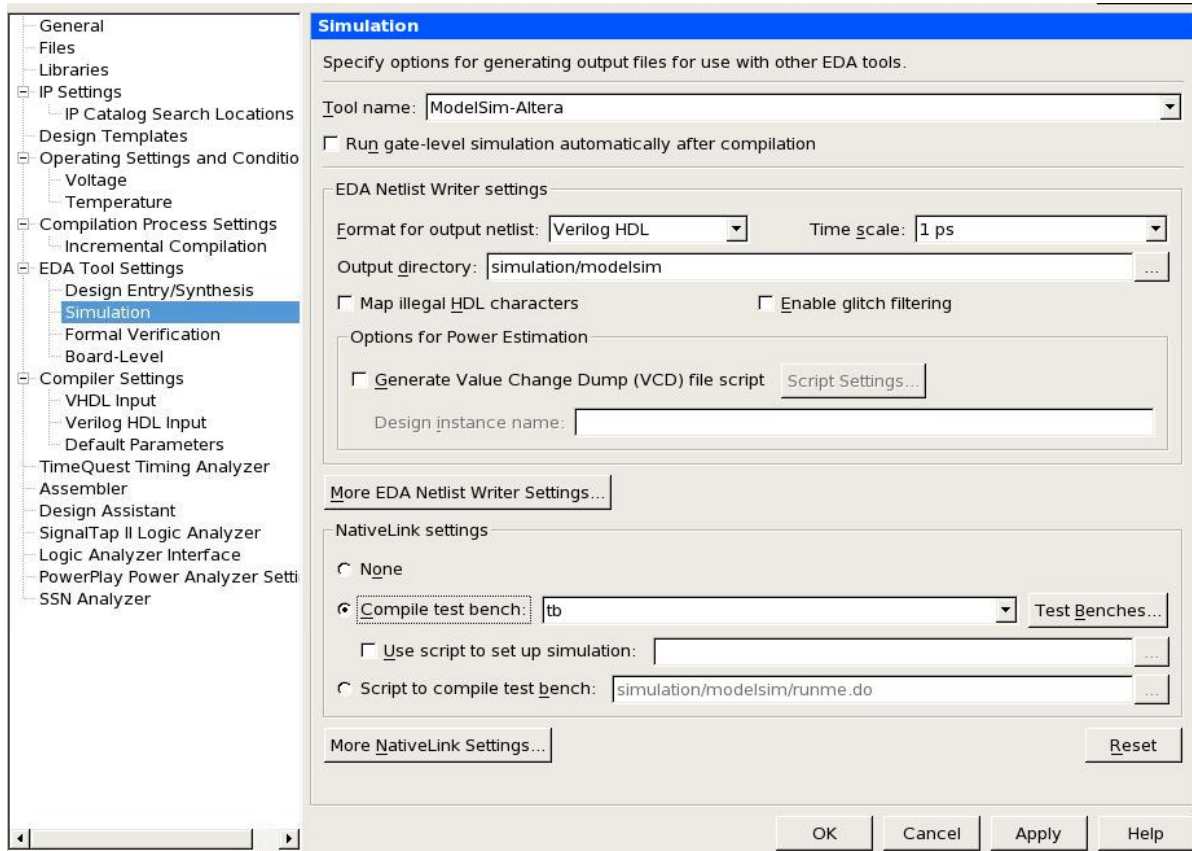
### Related Information

- [AN 747 Altera PHYLite Simulation Reference Design Files](#)
- [Getting Started with the Design Store](#)  
Guideline to download and install design examples from Design Store.

## Setting Up Simulation Environment

1. Follow the guidelines in [Getting Started with the Design Store](#) to download and install the reference design files.
2. Open the reference design .qpf file after successfully installing the design templates.
3. Click on **Assignments** -> **Settings....**
4. Select **EDA Tools Settings** -> **Simulation**.
5. At the Settings window, choose **Modelsim-Altera** for **Tool Name**. You may choose **VHDL**, **Verilog HDL** or **System Verilog** as the output netlist format.

Figure 2: Simulation Settings using EDA Tools in the Quartus Prime Software



6. Open dut\_INPUT.qsys file and make sure the IP has the same configuration shown below:

Figure 3: Configuration for dut\_INPUT Module

The image shows two side-by-side screenshots of the Altera PHYLite configuration tool. The left screenshot shows the 'Parameters' and 'I/O Settings' sections. The right screenshot shows the 'Group 0 Pin Settings', 'Group 0 Input Path Settings', 'Group 0 Output Path Settings', 'Group 0 General Data Settings', 'Group 0 General Strobe Settings', 'Group 0 OCT Settings', and 'Group 0 Timing Settings' sections.

**Parameters**  
Number of groups: 1

**General | Group 0**

**Clocks**  
Interface clock frequency: 800.0 MHz  
 Use core PLL reference clock connection  
 Use recommended PLL reference clock frequency  
PLL reference clock frequency: 200.0 MHz  
VCO clock frequency: 800.0 MHz  
Clock rate of user logic: Quarter  
 Specify additional output clocks based on existing PLL

**Dynamic Reconfiguration**  
 Use dynamic reconfiguration  
Interface ID: 0

**I/O Settings**  
I/O standard: SSTL-15 Class I

**Group 0 Parameter Settings**  
 Copy parameters from another group

**Group 0 Pin Settings**  
Pin type: Input  
Pin width: 4  
DDR/SDR: DDR

**Group 0 Input Path Settings**  
Read latency: 9 external interface clock cycles  
 Swap capture strobe polarity  
Capture strobe phase shift: 0 degrees

**Group 0 Output Path Settings**  
Write latency: 0 external interface clock cycles  
 Use output strobe  
Output strobe phase: 30 degrees

**Group 0 General Data Settings**  
Data configuration: Single ended

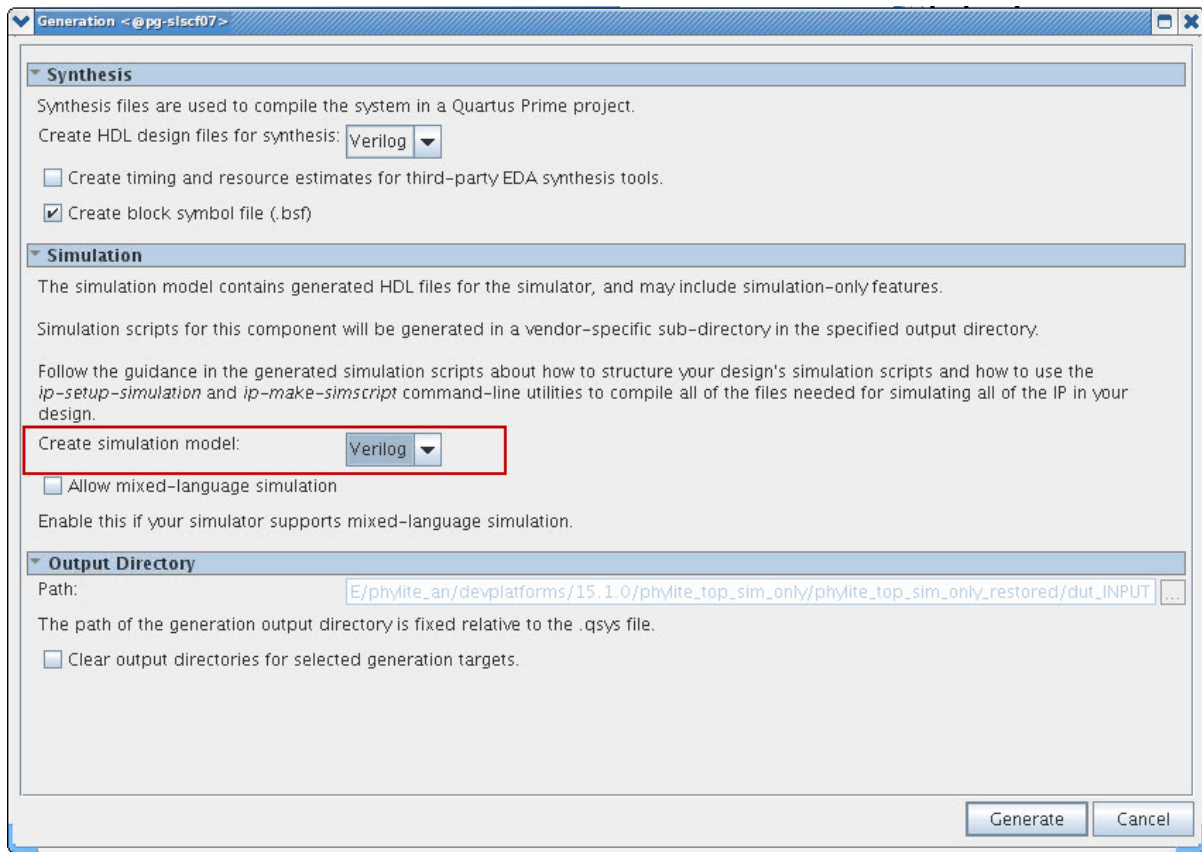
**Group 0 General Strobe Settings**  
Strobe configuration: Single ended  
 Use separate strobes

**Group 0 OCT Settings**  
OCT enable size: 1  
 Use Default OCT Values  
Input OCT Value: No termination  
Output OCT Value: No termination

**Group 0 Timing Settings**  
 Generate Input Delay Constraints for this group  
Input Strobe Setup Delay Constraint: 0.03 ns  
Input Strobe Hold Delay Constraint: 0.03 ns  
Inter Symbol Interference of the Read Channel: 0.09 ns

7. Make sure that the **Capture strobe phase shift** is set to **0** degrees to align the incoming data to strobe edge during data transfer.
8. Click **Generate HDL...** and select your desired simulation model format. Next, click **Generate** to generate the simulation model for the dut\_INPUT module. Click **Close** and **Finish** when the generation is complete.

Figure 4: Generating Simulation Model



9. From the Quartus® Prime software, open dut\_OUTPUT.qsys file and make sure the IP has the same configuration shown below:

以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：<https://d.book118.com/625001201344011224>