Altera PHYLite for Parallel Interfaces Loopback Reference Designs Application Note

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AN-747 Subscribe Send Feedback

This application note showcases loopback reference designs using the Altera PHYLite IP core.

This document is divided into three main segments:

1. A simple input/output PHYLite simulation reference design.
2. A simple input/output PHYLite with dynamic reconfiguration using Arria 10 devices hardware reference design.
3. Functional description for the modules and application used in both reference designs.

Simple Input/Output PHYLite Simulation Design Example

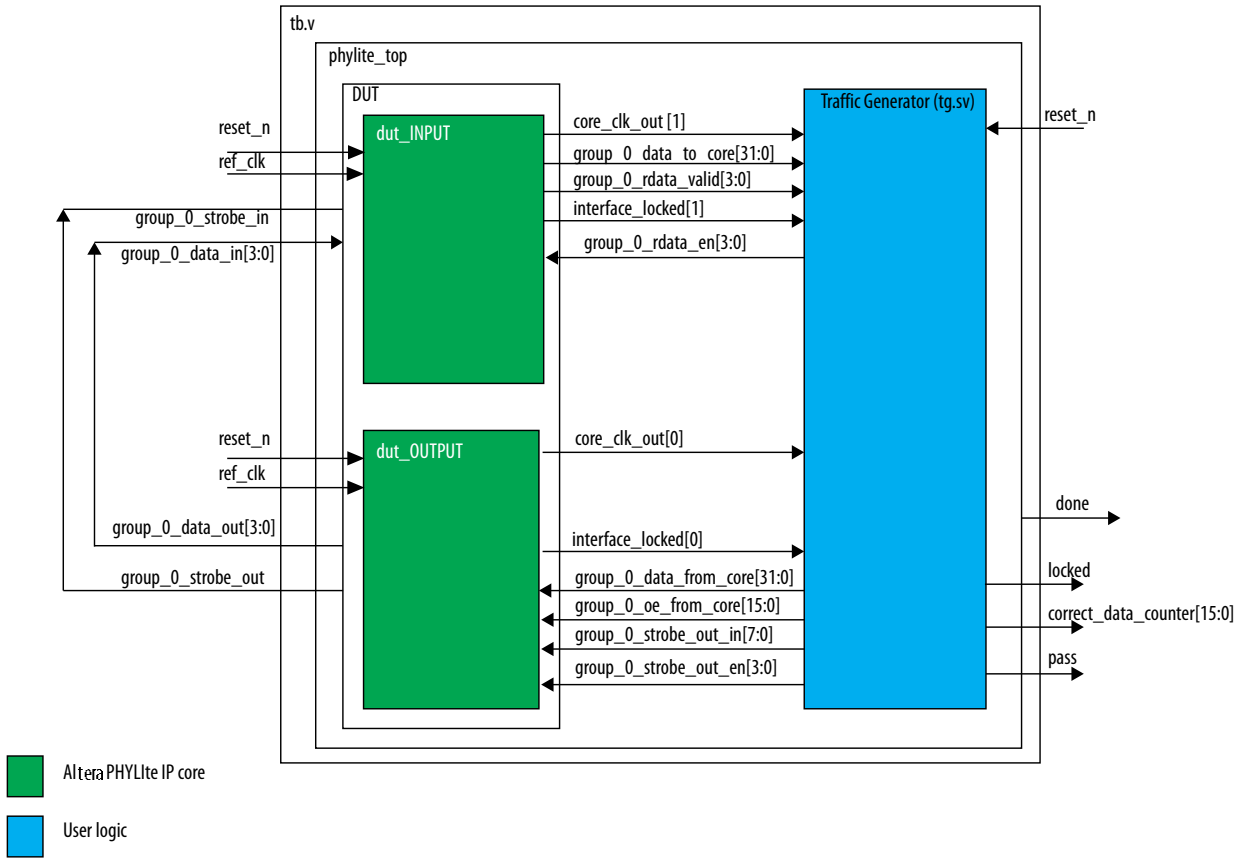
This section provides architecture description and user guide for the simulation reference design.

Simulation Design Example Architecture

The simulation reference design is a simple design that simulates the behavior of the Altera PHYLite IP core. This design consists of 2 main components:

- A device Under Test (DUT) module that includes two Altera PHYLite IP instances.
- A traffic generator module

Figure 1: Simulation Reference Design Block Diagram



Simulation Reference Design User Guide

Follow these steps to setup and run the simulation reference design.

Requirements

The following are the requirements to run the simulation reference design:

- Quartus Prime Design Suite® versions 15.1
- Simulation design example phylite_top_sim_only.par

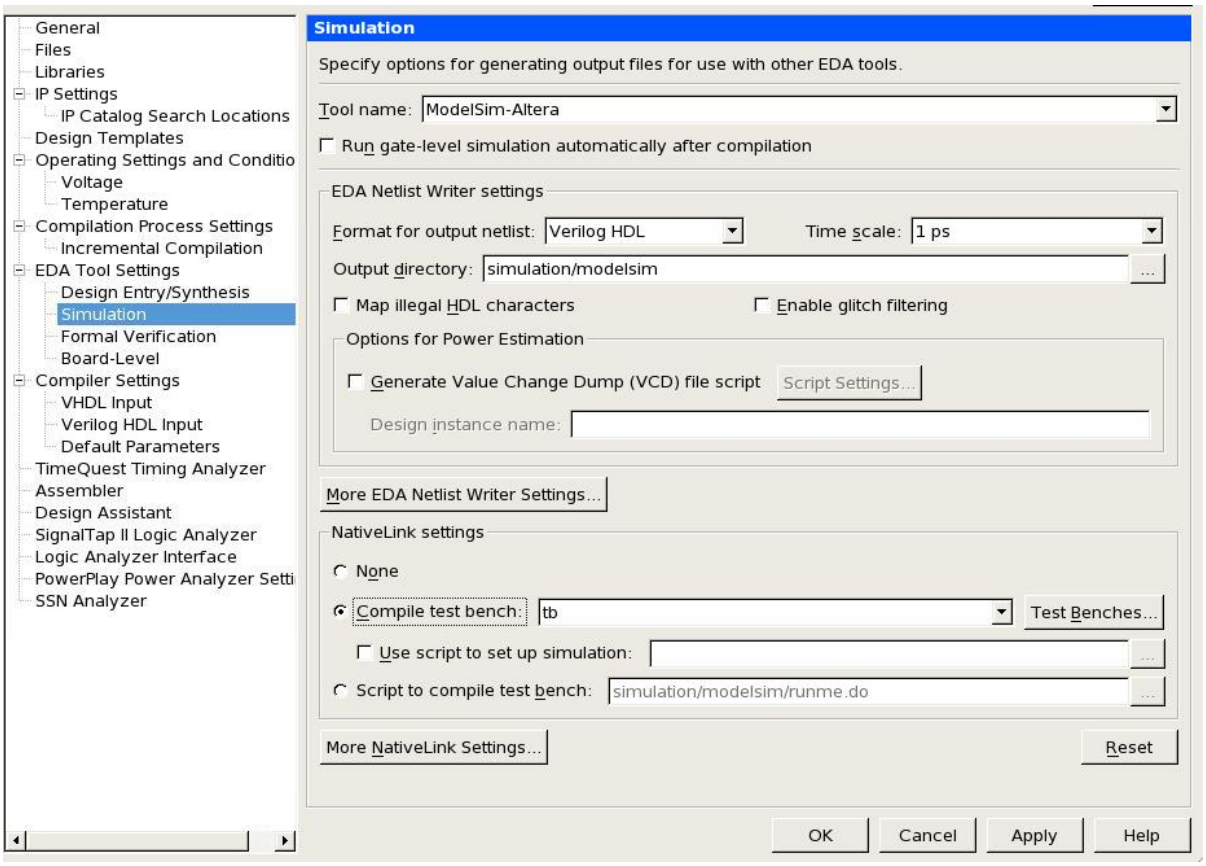
Related Information

- **AN 747 Altera PHYLite Simulation Reference Design Files**
- **Getting Started with the Design Store**
  Guideline to download and install design examples from Design Store.

Setting Up Simulation Environment

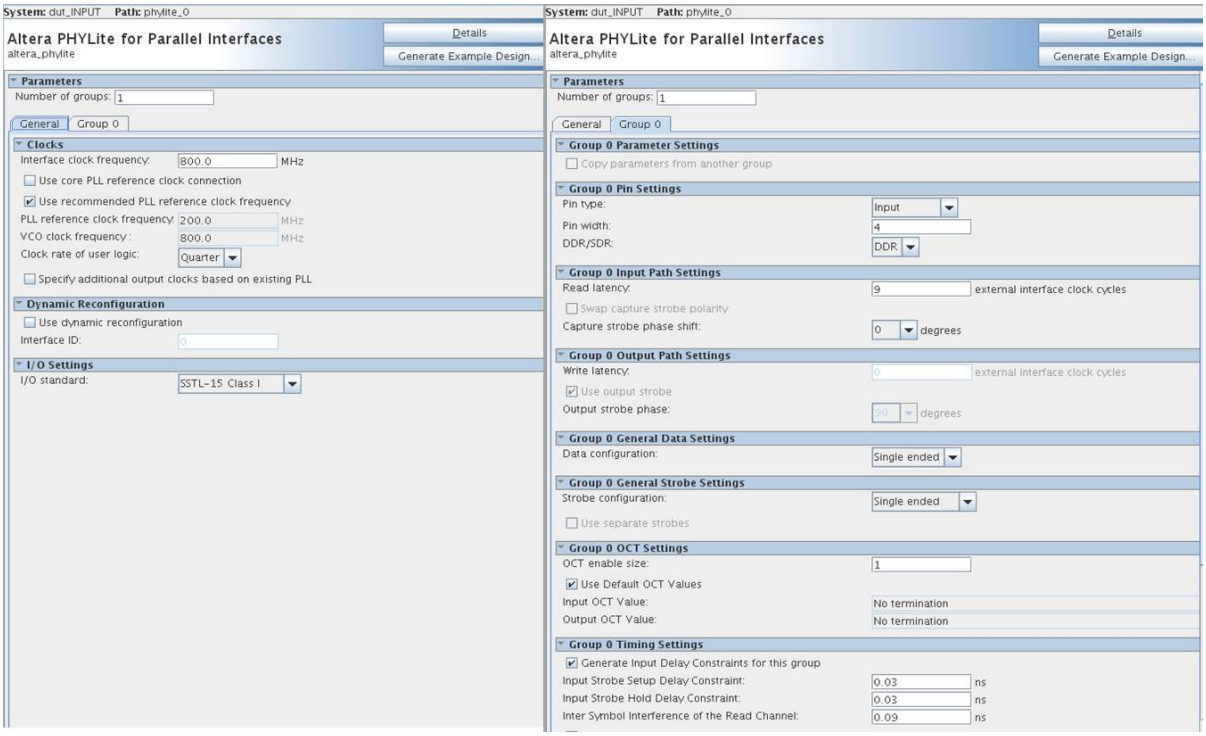
1. Follow the guidelines in **Getting Started with the Design Store** to download and install the reference design files.
2. Open the reference design .qpf file after successfully installing the design templates.
3. Click on **Assignments** -> **Settings...**.
4. Select **EDA Tools Settings** -> **Simulation**.
5. At the Settings window, choose **Modelsim-Altera** for **Tool Name**. You may choose **VHDL**, **Verilog HDL** or **System Verilog** as the output netlist format.

Figure 2: Simulation Settings using EDA Tools in the Quartus Prime Software



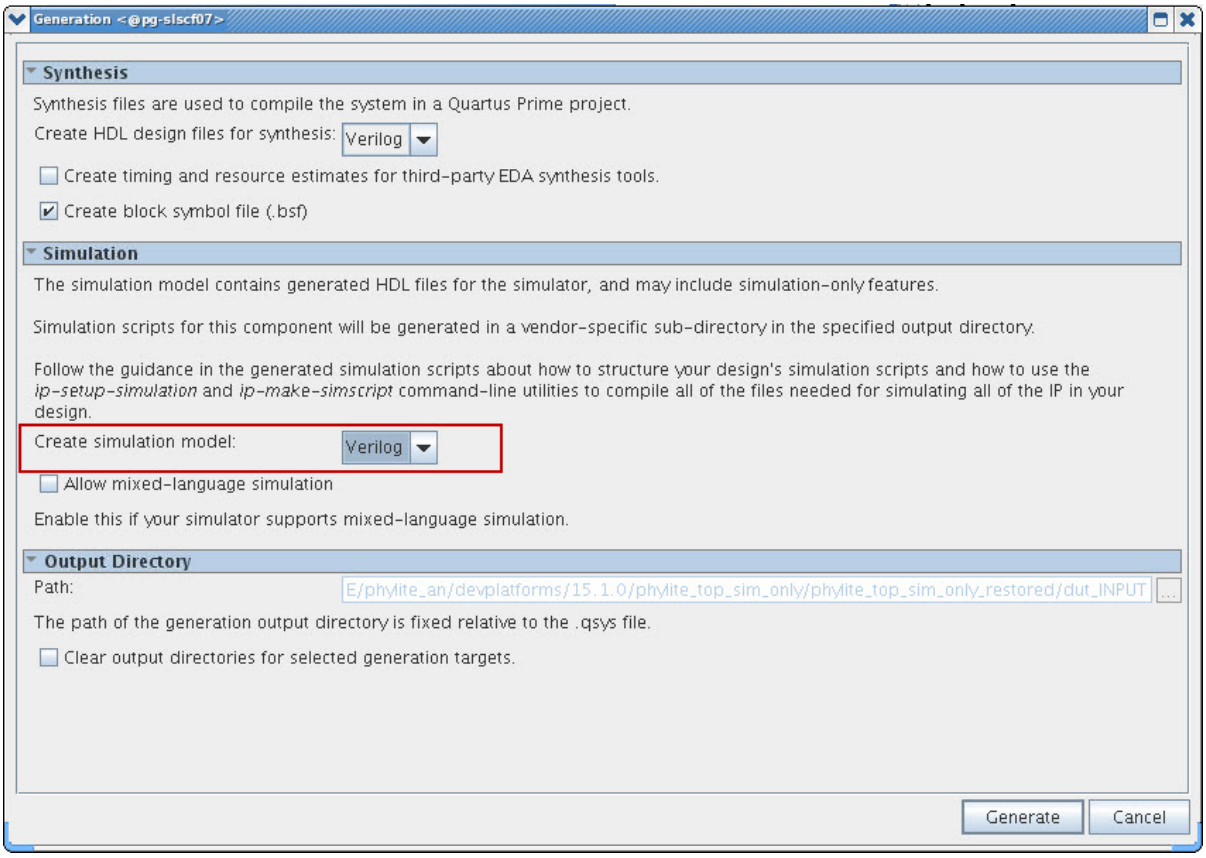
6. Open dut_INPUT.qsys file and make sure the IP has the same configuration shown below:

Figure 3: Configuration for dut_INPUT Module



7. Make sure that the **Capture strobe phase shift** is set to **0** degrees to align the incoming data to strobe edge during data transfer.
8. Click **Generate HDL...** and select your desired simulation model format. Next, click **Generate** to generate the simulation model for the dut_INPUT module. Click **Close** and **Finish** when the generation is complete.

Figure 4: Generating Simulation Model



9. From the Quartus® Prime software, open dut_OUTPUT.qsys file and make sure the IP has the same configuration shown below: