Ultra Small Voltage Detector with High Precision Delay Circuit and Manual Reset Function

■GENERAL DESCRIPTION

XC6127 series is ultra small highly accurate voltage detector with delay circuit built-in.

The device includes a highly accurate reference voltage source, manufactured using CMOS process technology and laser trimming technologies, it maintains high accuracy, low power consumption, and accurate releases delay time over the full operation temperature range.

The release delay time periods are internally set in a range from 50ms to 800ms.

Moreover, with the manual reset function, reset can be asserted at any time.

The device is available in both CMOS and N-channel open drain output configurations. Also detect logic is available in both RESETB (Active Low) and RESET (Active High).

Ultra small package USPN-4 is ideally suited for small design of portable devices and high densely mounting applications. The conventional packages SSOT-24, SOT-25 is also available for upper compatible replacements.

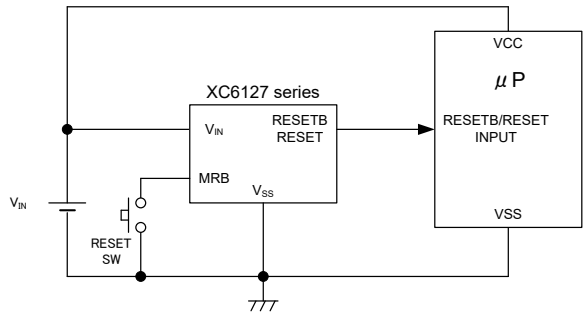
■APPLICATIONS

- Microprocessor logic reset circuitry
- System battery life and charge voltage monitors
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure Detection
- Delay circuit

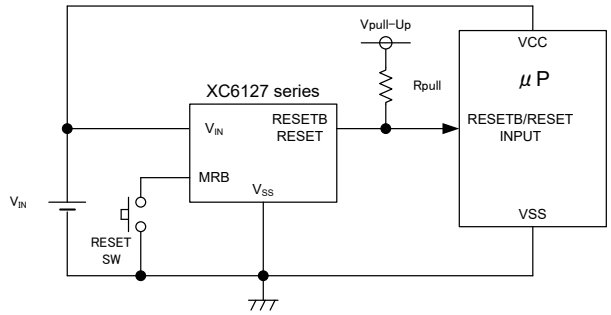
■FEATURES

High Accuracy	:	±0.8% (25℃)
Temperature Characteristics	:	±50ppm/℃
Low Power Consumption	:	0.6μA TYP. (Detect: V_{DF}=1.8V, V_{IN}=1.62V)
		0.7μA TYP. (Release: V_{DF}=1.8V, V_{IN}=1.98V)
Operating Voltage Range	:	0.7V ~ 6.0V
Detect Voltage Range	:	1.5V ~ 5.5V (0.1V increments)
Manual Reset Input	:	MRB Pin (Built-in Pull-up resistance)
Output Configuration	:	N-channel open drain or CMOS
Output Logic	:	RESETB (Active Low)
		RESET (Active High)
Release Delay Time	:	50ms/100ms/200ms/400ms/800ms±15%
Operating Ambient Temperature	:	-40℃ ~ 85℃
Packages	:	USPN-4, SSOT-24, SOT-25
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

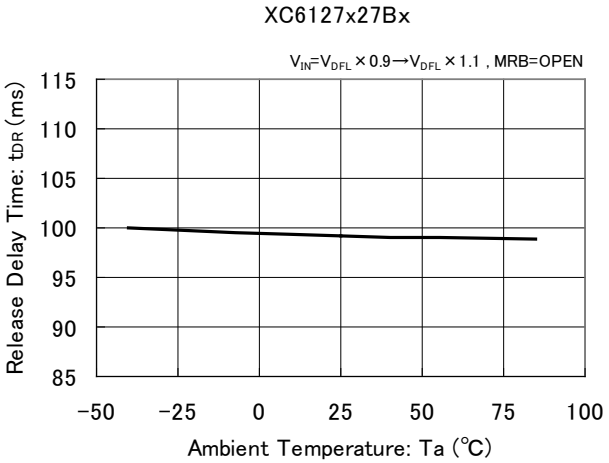


CMOS output



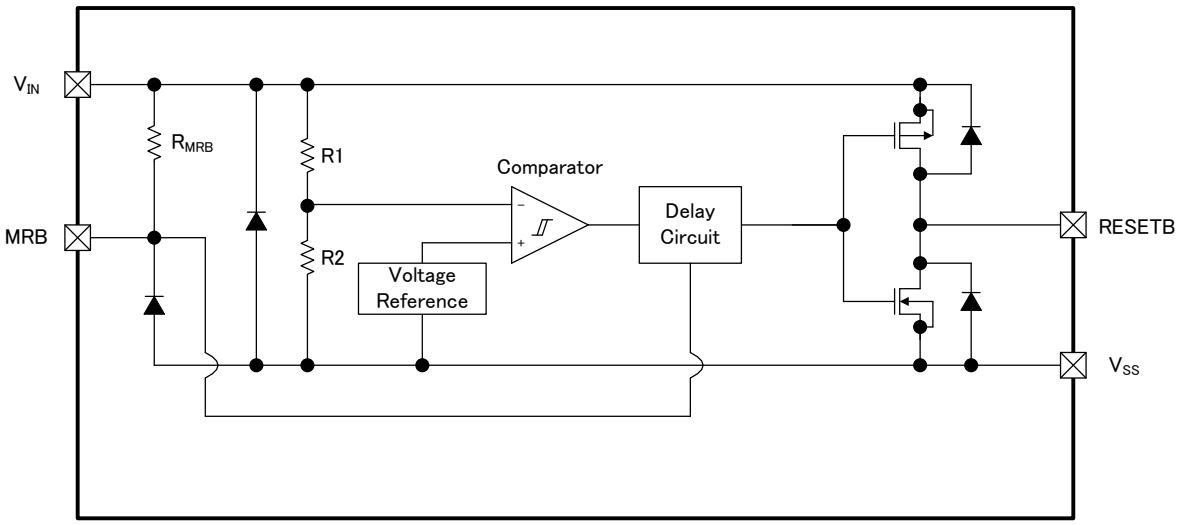
N-ch open drain output

■ TYPICAL PERFORMANCE CHARACTERISTICS



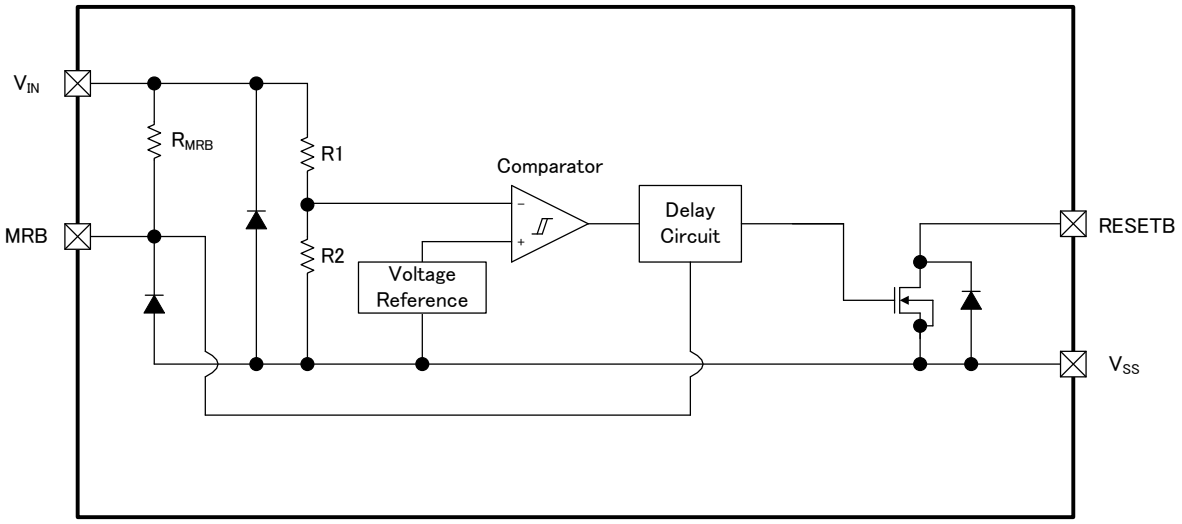
■BLOCK DIAGRAMS

1) XC6127 Series, Type CxxA/CxxB/CxxC/CxxD/CxxE (CMOS Output, Output Logic: Active Low)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

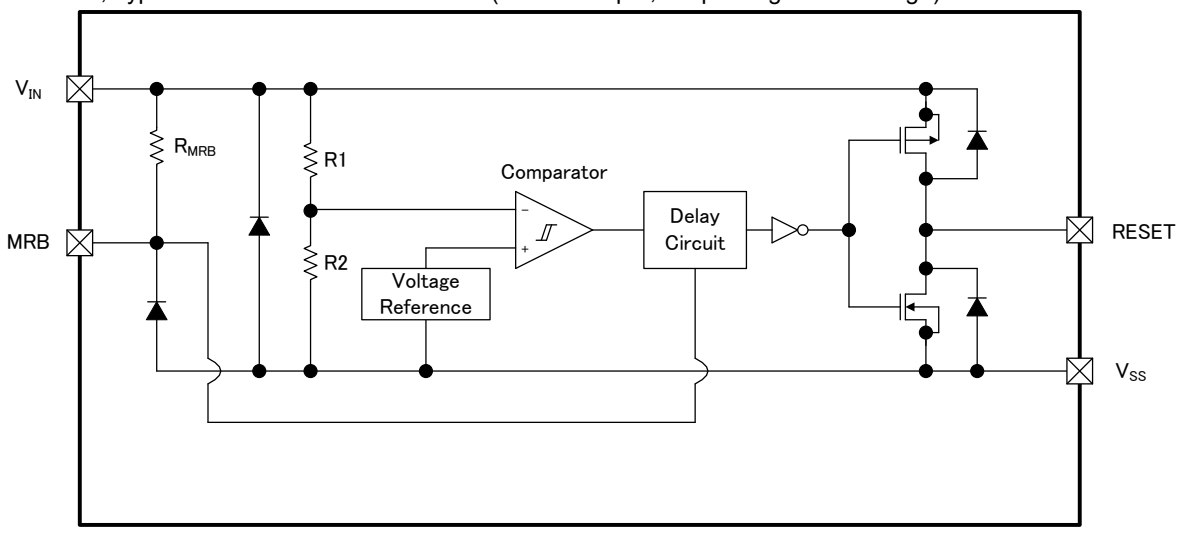
2) XC6127 Series, Type NxxA/NxxB/NxxC/NxxD/NxxE (N-ch Open Drain Output, Output Logic: Active Low)



* Diodes inside the circuits are ESD protection diodes

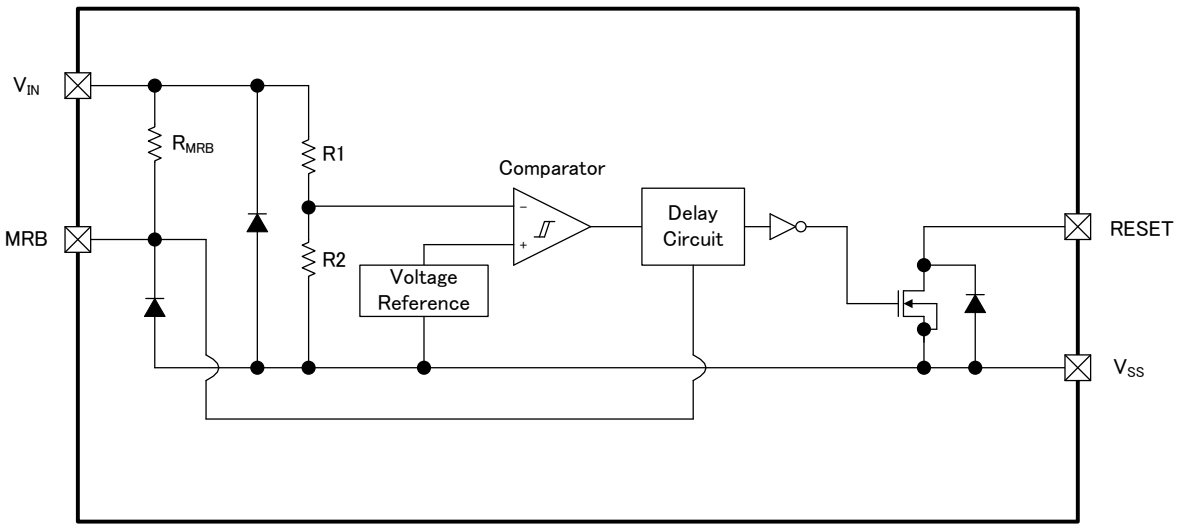
■BLOCK DIAGRAMS (Continued)

3) XC6127 Series, Type CxxF/CxxG/CxxH/CxxJ/CxxK (CMOS Output, Output Logic: Active High)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

4) XC6127 Series, Type NxxF/NxxG/NxxH/NxxJ/NxxK (N-ch Open Drain Output, Output Logic: Active High).



* Diodes inside the circuits are ESD protection diodes.

■PRODUCT CLASSIFICATION

●Ordering Information

XC6127①②③④⑤⑥-⑦(*1)

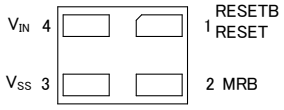
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
②③	Detect Voltage	15 ~ 55	e.g. 2.7V → ②=2, ③=7
④	Type	A	Reset Active Low, Release Delay Time: 50ms
		B	Reset Active Low, Release Delay Time: 100ms
		C	Reset Active Low, Release Delay Time: 200ms
		D	Reset Active Low, Release Delay Time: 400ms
		E	Reset Active Low, Release Delay Time: 800ms
		F	Reset Active High, Release Delay Time: 50ms
		G	Reset Active High, Release Delay Time: 100ms
		H	Reset Active High, Release Delay Time: 200ms
		J	Reset Active High, Release Delay Time: 400ms
		K	Reset Active High, Release Delay Time: 800ms
⑤⑥-⑦(*1)	Packages (Order Unit)	7R-G	USPN-4 (5,000pcs/Reel)
		MR-G	SOT-25 (3,000pcs/Reel)
		NR-G	SSOT-24 (3,000pcs/Reel)

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

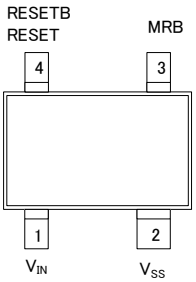
2) Selection Guide

TYPE	Release Delay Time	Output Logic
A	50ms	Active Low
B	100ms	Active Low
C	200ms	Active Low
D	400ms	Active Low
E	800ms	Active Low
F	50ms	Active High
G	100ms	Active High
H	200ms	Active High
J	400ms	Active High
K	800ms	Active High

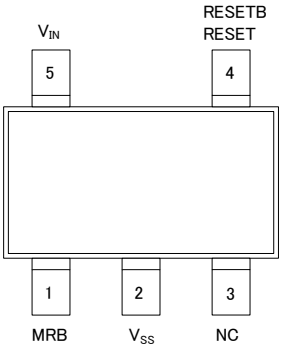
■PIN CONFIGURATION



USPN-4
(BOTTOM VIEW)



SSOT-24
(TOP VIEW)



SOT-25
(TOP VIEW)

■PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTIONS
USPN-4	SSOT-24	SOT-25		
1	4	4	RESETB	Signal Output (Active Low) (*1)
			RESET	Signal Output (Active High) (*2)
2	3	1	MRB	Manual Reset Input
3	2	2	V_{SS}	Ground
4	1	5	V_{IN}	Power Input
-	-	3	NC	No Connection

(*1) Type A ~ E (Refer to the ④ in Ordering Information table)
(*2) Type F ~ K (Refer to the ④ in Ordering Information table)

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
MRB	L	Forced Reset
	H	Normal Operation
	OPEN	Normal Operation

■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	V_{SS} - 0.3 ~ V_{SS} + 6.5	V
MRB Input Voltage		V_{MRB}	V_{SS} ~ V_{SS}+6.5	V
Output Current		(*1)	20	mA
Output Voltage	XC6127C (*2)	(*4)	V_{SS} - 0.3 ~ V_{IN} + 0.3 ≦ V_{SS} + 6.5	V
	XC6127N (*3)		V_{SS} - 0.3 ~ V_{SS} + 6.5	
Power Dissipation (Ta=25℃)	USPN-4	Pd	100	mW
			600 (40mm x 40mm Standard board) (*5)	
	SOT-25		250	
			600 (40mm x 40mm Standard board) (*5)	
			760 (JESD51-7 board)) (*5)	
	SSOT-24		150	
			500 (40mm x 40mm Standard board) (*5)	
			680 (JESD51-7 board) (*5)	
Operating Ambient Temperature		Topr	-40 ~ 85	℃
Storage Temperature		Tstg	-55 ~ 125	℃

(*1) SYMBOL is different for each product.
I_{RBOUT}: Type XC6127CxxA/CxxB/CxxC/CxxD/CxxE, Type XC6127NxxA/NxxB/NxxC/NxxD/NxxE
I_{ROUT}: Type XC6127CxxF/CxxG/CxxH/CxxJ/CxxK, Type XC6127NxxF/NxxG/NxxH/NxxJ/NxxK
(*2) CMOS Output
(*3) N-ch Open Drain Output
(*4) SYMBOL is different for each product.
V_{RESETB}: Type XC6127CxxA/CxxB/CxxC/CxxD/CxxE, Type XC6127NxxA/NxxB/NxxC/NxxD/NxxE
V_{RESET}: Type XC6127CxxF/CxxG/CxxH/CxxJ/CxxK, Type XC6127NxxF/NxxG/NxxH/NxxJ/NxxK
(*5) This power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■ELECTRICAL CHARACTERISTICS

●XC6127CxxA/CxxB/CxxC/CxxD/CxxE, XC6127NxxA/NxxB/NxxC/NxxD/NxxE (Output Logic: Active Low)

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUI
Operating Voltage	V_{IN}	$V_{DF(T)}$(*1)=1.5 ~ 5.5V, MRB=OPEN (*2)	0.7 (*3)		6.0	V	–
Detect Voltage	V_{DFL}	$V_{DF(T)}$=1.5 ~ 5.5V, MRB=OPEN	$V_{DF(T)}$×0.992	$V_{DF(T)}$	$V_{DF(T)}$×1.008	V	①
			E-1(*4)				
Hysteresis Width	V_{HYS}		V_{DFL}×0.02	V_{DFL}×0.05	V_{DFL}×0.08	V	①
Supply Current 1	I_{SS1}	V_{IN}=V_{DFL}×0.9 , MRB=OPEN				μA	②
		$V_{DF(T)}$=1.5 ~ 1.8V	-	0.6	1.4		
		$V_{DF(T)}$=1.9 ~ 3.0V	-	0.7	1.6		
		$V_{DF(T)}$=3.1 ~ 5.5V	-	1.0	1.9		
Supply Current 2	I_{SS2}	V_{IN}=V_{DFL}×1.1(*5) , MRB=OPEN				μA	②
		$V_{DF(T)}$=1.5 ~ 1.8V	-	0.7	1.6		
		$V_{DF(T)}$=1.9 ~ 3.0V	-	0.8	1.9		
		$V_{DF(T)}$=3.1 ~ 5.5V	-	1.1	2.35		
RESETB Output Current	I_{RBOUT1}	V_{IN}=0.7V, V_{RESETB}=0.5V(Nch) , MRB=OPEN	0.014	0.2	-	mA	③
		V_{IN}=1.0V, V_{RESETB}=0.5V(Nch) , MRB=OPEN	0.5	1.6	-		
		V_{IN}=2.0V(*6), V_{RESETB}=0.5V(Nch) , MRB=OPEN	4.4	7.0	-		
		V_{IN}=3.0V(*7), V_{RESETB}=0.5V(Nch) , MRB=OPEN	7.0	9.0	-		
		V_{IN}=4.0V(*8), V_{RESETB}=0.5V(Nch) , MRB=OPEN	8.5	11.0	-		
		V_{IN}=5.0V(*9), V_{RESETB}=0.5V(Nch) , MRB=OPEN	9.0	12.0	-		
	I_{RBOUT2}(*10)	V_{IN}=6.0V, V_{RESETB}=5.5V(Pch) , MRB=OPEN	-	-4.5	-3.0	mA	③
RESETB Leakage Current CMOS Output(Pch)	I_{LEAK}	V_{IN}=V_{DFL}×0.9, V_{RESETB}=0V , MRB=OPEN	-	-0.01	-	μA	③
RESETB Leakage Current Nch Open Drain Output		V_{IN}=6.0V, V_{RESETB}=6.0V , MRB=OPEN	-	0.01	0.15	μA	
Temperature Characteristics	ΔV_{DFL}/(ΔTopr・V_{DFL})	-40℃≦Topr≦85℃	-	±50	-	ppm/℃	①
Detect Delay Time(*11)	t_{DF}	V_{IN}=V_{DFL}×1.1→V_{DFL}×0.9(*11), MRB=OPEN	-	-	100	μs	④
Release Delay Time(*12)	t_{DR}	V_{IN}=V_{DFL}×0.9→V_{DFL}×1.1(*12), MRB=OPEN	E-2 (*13)			ms	④
MRB "Low" Level Voltage(*14)	V_{MRL}	V_{DFL}×1.1≦V_{IN}≦6.0V	V_{SS}	-	0.3	V	⑤
MRB "High" Level Voltage(*14)	V_{MRH}	V_{DFL}×1.1≦V_{IN}≦6.0V	1.0	-	6.0	V	⑤
MRB pull-up Resistance	R_{MRB}		0.4	0.8	3.0	MΩ	⑥
Minimum MRB Pulse Width	T_{MRB}	V_{IN}=6.0V, Applied pulse to MRB pin,	150	-	-	ns	⑦

(*1) $V_{DF(T)}$: Nominal detect voltage
(*2) For the N-ch Open Drain, Rpull=100kΩ, Vpull-Up=V_{IN}
Rpull: An External Pull-up resistor
Vpull-Up: Pull-up Voltage
(*3) V_{IN} voltage for V_{OUT}≦0.3V is under detect state.
(*4) For the detail value, please refer to "Voltage Table" in P10.
(*5) $V_{DF(T)}$ = 5.5V where V_{IN}=6.0V
(*6) For $V_{DF(T)}$＞2.0V products.
(*7) For $V_{DF(T)}$＞3.0V products.
(*8) For $V_{DF(T)}$＞4.0V products.
(*9) For $V_{DF(T)}$＞5.0V products.
(*10) For the XC6127C (CMOS output)
(*11) A time between V_{IN}=V_{DFL} and V_{RESETB}=V_{DFL}×0.45 when V_{IN} falls.
(*12) A time between V_{IN}=V_{DFL}+V_{HYS} and V_{RESETB}=V_{DFL}×0.55 when V_{IN} rises.
(*13) For the detail value, please refer to "Release Delay Time" in P11.
(*14) For MRB pin, please do not apply the voltage below V_{SS}.

■ELECTRICAL CHARACTERISTICS (Continued)

●XC6127CxxF/CxxG/CxxH/CxxJ/CxxK, XC6127NxxF/NxxG/NxxH/NxxJ/NxxK (Output Logic: Active High)

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Operating Voltage	V_{IN}	$V_{DF(T)}$(*1)=1.5 ~ 5.5V, MRB=OPEN(*2)	0.7 (*3)		6.0	V	–
Detect Voltage	V_{DFH}	$V_{DF(T)}$=1.5 ~ 5.5V, MRB=OPEN	$V_{DF(T)}$×0.992	$V_{DF(T)}$	$V_{DF(T)}$×1.008	V	①
			E-1(*4)				
Hysteresis Width	V_{HYS}		V_{DFH}×0.02	V_{DFH}×0.05	V_{DFH}×0.08	V	①
Supply Current 1	I_{SS1}	V_{IN}=V_{DFH}×0.9, MRB=OPEN				μA	②
		$V_{DF(T)}$=1.5 ~ 1.8V	-	0.6	1.4		
		$V_{DF(T)}$=1.9 ~ 3.0V	-	0.7	1.6		
		$V_{DF(T)}$=3.1 ~ 5.5V	-	1.0	1.9		
Supply Current 2	I_{SS2}	V_{IN}=V_{DFH}×1.1(*5) , MRB=OPEN				μA	②
		$V_{DF(T)}$=1.5 ~ 1.8V	-	0.7	1.6		
		$V_{DF(T)}$=1.9 ~ 3.0V	-	0.8	1.9		
		$V_{DF(T)}$=3.1 ~ 5.5V	-	1.1	2.35		
RESET Output Current	I_{ROUT1}	V_{IN}=1.65V(*6), V_{RESET}=0.5V(Nch) , MRB=OPEN	0.5	1.6	-	mA	③
		V_{IN}=2.0V(*7), V_{RESET}=0.5V(Nch) , MRB=OPEN	4.4	7.0	-		
		V_{IN}=3.0V(*8), V_{RESET}=0.5V(Nch) , MRB=OPEN	7.0	9.0	-		
		V_{IN}=4.0V(*9), V_{RESET}=0.5V(Nch) , MRB=OPEN	8.5	11.0	-		
		V_{IN}=5.0V(*10), V_{RESET}=0.5V(Nch) , MRB=OPEN	9.0	12.0	-		
		V_{IN}=6.0V, V_{RESET}=0.5V(Nch) , MRB=OPEN	9.0	12.0	-		
	I_{ROUT2} (*11)	V_{IN}=0.7V, V_{RESET}=0.2V(Pch) , MRB=OPEN	-	-0.07	-0.001	mA	③
		V_{IN}=1.0V, V_{RESET}=0.5V(Pch) , MRB=OPEN	-	-0.4	-0.09		
		V_{IN}=2.0V(*12), V_{RESET}=1.5V(Pch) , MRB=OPEN	-	-2.0	-1.3		
		V_{IN}=3.0V(*13), V_{RESET}=2.5V(Pch) , MRB=OPEN	-	-3.0	-1.8		
		V_{IN}=4.0V(*14), V_{RESET}=3.5V(Pch) , MRB=OPEN	-	-4.0	-2.5		
		V_{IN}=5.0V(*15), V_{RESET}=4.5V(Pch) , MRB=OPEN	-	-4.5	-3.0		
RESET Leakage Current: CMOS Output (P-ch)	I_{LEAK}	V_{IN}=6.0V, V_{RESET}=0V, MRB=OPEN	-	-0.01	-	μA	③
RESET Leakage Current: N-ch Open Drain Output		V_{IN}=V_{DFH}×0.9, V_{RESET}=6.0V, MRB=OPEN	-	0.01	0.15	μA	
Temperature Characteristics	ΔV_{DFH}/ (ΔTopr·V_{DFH})	-40℃≦Topr≦85℃	-	±50	-	ppm/℃	①
Detect Delay Time(*16)	t_{DF}	V_{IN}=V_{DFH}×1.1→V_{DFH}×0.9(*16), MRB=OPEN	-	-	E-3(*17)	μs	④
Release Delay Time(*18)	t_{DR}	V_{IN}=V_{DFH}×0.9→V_{DFH}×1.1(*18), MRB=OPEN	E-2(*19)			ms	④
MRB "Low" Level Voltage(*20)	V_{MRL}	V_{DFH}×1.1≦V_{IN}≦6.0V	V_{SS}	-	0.3	V	⑤
MRB "High" Level Voltage(*20)	V_{MRH}	V_{DFH}×1.1≦V_{IN}≦6.0V	1.0	-	6.0	V	⑤
MRB pull-up Resistance	R_{MRB}		0.4	0.8	3.0	MΩ	⑥
Minimum MRB Pulse Width	T_{MRB}	V_{IN}=6.0V, Applied pulse to MRB pin, 6.0V→0V	150	-	-	ns	⑦

■ELECTRICAL CHARACTERISTICS (Continued)

(*1) $V_{DF\ (T)}$: Nominal detect voltage
(*2) For the N-ch Open Drain, Rpull=100kΩ, Vpull-Up=V_{IN}
Rpull: An External Pull-up resistor
Vpull-Up: Pull-up Voltage
(*3) V_{IN} voltage for $V_{OUT} \geqq 0.4V$ is under detect state.
(*4) For the detail value, please refer to “Voltage Table” in P10.
(*5) $V_{DF\ (T)}$ = 5.5V where V_{IN}=6.0V
(*6) For $V_{DF\ (T)}$ =1.5V products.
(*7) For $V_{DF(T)} \leqq 1.8V$ products.
(*8) For VDF(T)≦2.7V products.
(*9) For $V_{DF(T)} \leqq 3.6V$ products.
(*10) For $V_{DF(T)} \leqq 4.6V$ products.
(*11) For the XC6127C (CMOS output)
(*12) For $V_{DF(T)} > 2.0V$ products.
(*13) For $V_{DF(T)} > 3.0V$ products.
(*14) For $V_{DF(T)} > 4.0V$ products.
(*15) For $V_{DF(T)} > 5.0V$ products.
(*16) A time between $V_{IN}=V_{DFH}$ and $V_{RESET}=V_{DFH} \times 0.45$ when V_{IN} falls.
(*17) For the detail value, please refer to “Detect Delay Time” in P11.
(*18) A time between $V_{IN}=V_{DFH}+V_{HYS}$ and $V_{RESET}=V_{DFH} \times 0.55$ when V_{IN} rises.
(*19) For the detail value, please refer to “Release Delay Time” in P11.
(*20) For MRB pin, please do not apply the voltage below V_{SS}.

■ELECTRICAL CHARACTERISTICS (Continued)

Voltage Table 1

NOMINAL DETECT VOLTAGE (V)	DETECT VOLTAGE (V) E-1	
$V_{DF(T)}$	V_{DFL} or V_{DFH}	
	MIN.	MAX.
1.50	1.4880	1.5120
1.60	1.5872	1.6128
1.70	1.6864	1.7136
1.80	1.7856	1.8144
1.90	1.8848	1.9152
2.00	1.9840	2.0160
2.10	2.0832	2.1168
2.20	2.1824	2.2176
2.30	2.2816	2.3184
2.40	2.3808	2.4192
2.50	2.4800	2.5200
2.60	2.5792	2.6208
2.70	2.6784	2.7216
2.80	2.7776	2.8224
2.90	2.8768	2.9232
3.00	2.9760	3.0240
3.10	3.0752	3.1248
3.20	3.1744	3.2256
3.30	3.2736	3.3264
3.40	3.3728	3.4272
3.50	3.4720	3.5280
3.60	3.5712	3.6288
3.70	3.6704	3.7296
3.80	3.7696	3.8304
3.90	3.8688	3.9312
4.00	3.9680	4.0320

Voltage Table 2

NOMINAL DETECT VOLTAGE (V)	DETECT VOLTAGE (V) E-1	
$V_{DF(T)}$	V_{DFL} or V_{DFH}	
	MIN.	MAX.
4.10	4.0672	4.1328
4.20	4.1664	4.2336
4.30	4.2656	4.3344
4.40	4.3648	4.4352
4.50	4.4640	4.5360
4.60	4.5632	4.6368
4.70	4.6624	4.7376
4.80	4.7616	4.8384
4.90	4.8608	4.9392
5.00	4.9600	5.0400
5.10	5.0592	5.1408
5.20	5.1584	5.2416
5.30	5.2576	5.3424
5.40	5.3568	5.4432
5.50	5.4560	5.5440

■ELECTRICAL CHARACTERISTICS (Continued)

Release Delay Time Table

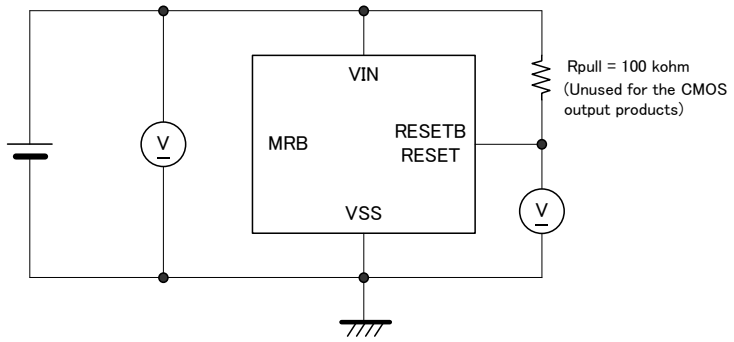
TYPE	RELEASE DELAY TIME (ms) E-2		
	t_{DR}		
	MIN.	TYP.	MAX.
XC6127CxxA / XC6127NxxA	42.5	50	57.5
XC6127CxxB / XC6127NxxB	85	100	115
XC6127CxxC / XC6127NxxC	170	200	230
XC6127CxxD / XC6127NxxD	340	400	460
XC6127CxxE / XC6127NxxE	680	800	920
XC6127CxxF / XC6127NxxF	42.5	50	57.5
XC6127CxxG / XC6127NxxG	85	100	115
XC6127CxxH / XC6127NxxH	170	200	230
XC6127CxxJ / XC6127NxxJ	340	400	460
XC6127CxxK / XC6127NxxK	680	800	920

Detect Delay Time Table

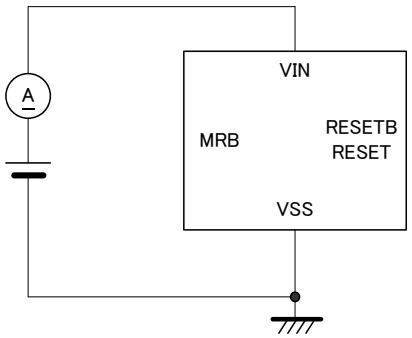
TYPE	DETECT DELAY TIME (μs) E-3
	t_{DF}
	MAX.
XC6127CxxF/CxxG/CxxH/CxxJ/CxxK	100
XC6127NxxF/NxxG/NxxH/NxxJ/NxxK	200

■TEST CIRCUITS

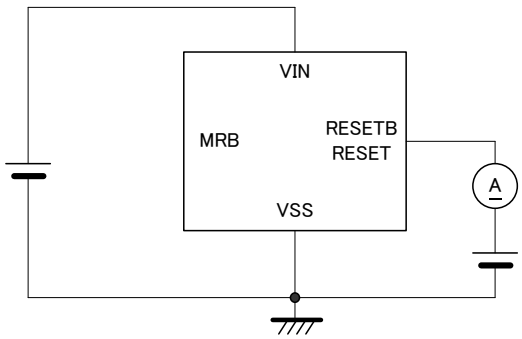
Circuit ①



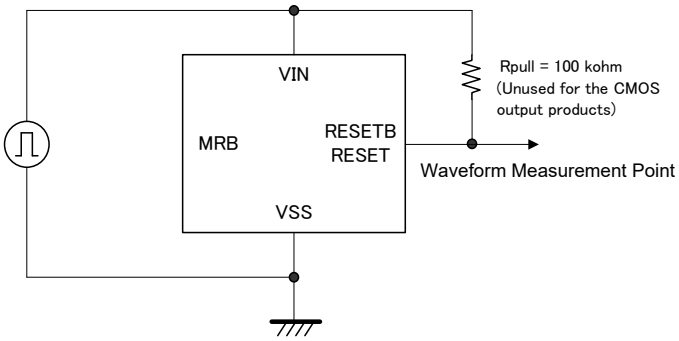
Circuit ②



Circuit ③

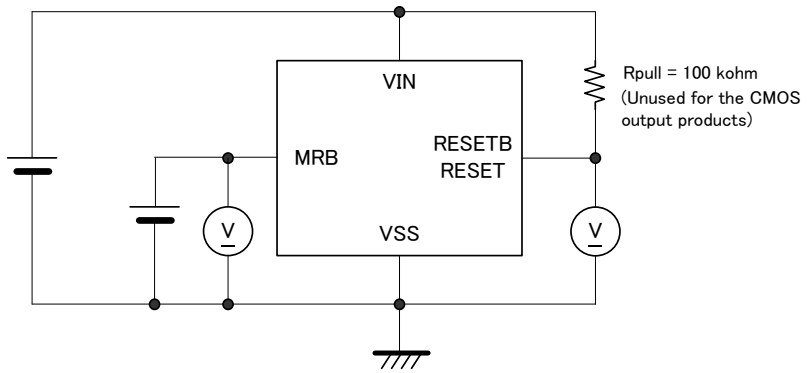


Circuit ④

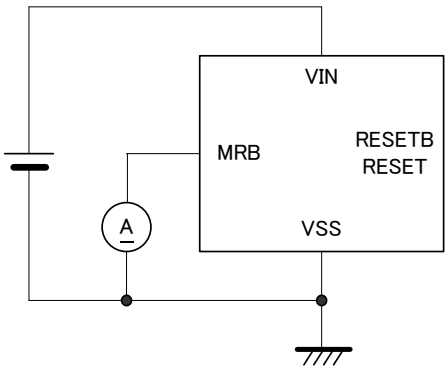


■TEST CIRCUITS (Continued)

Circuit ⑤



Circuit ⑥



Circuit ⑦