

Conventions .....	5
Definitions .....	5
References:.....	5
Revision History .....	5
1. Introduction.....	6
1.1. OVERVIEW.....	6
2. SL811HS Host or Slave MODE .....	7
2.1. OVERVIEW.....	7
2.2. HARDWARE REQUIREMENTS.....	7
2.2.1 External Controller and USB connectors .....	7
2.3. POWER ON AND RESET MODE .....	7
2.4. SWITCHING LOGIC.....	9
2.5. SOFTWARE INITIALIZATION.....	10
2.5.1 Initialization from Host to Slave.....	11
2.5.2 Initialization from Slave to Host.....	12
2.6. M/S PIN (PIN27/PIN40) .....	13
2.7. PULL-UP/DOWN REGISTERS ON USB LINES .....	13
2.8. HOST/SLAVE DETECTOR .....	13
3. Programming Information .....	15
3.1. HOST AND DEVICE PROGRAMMING .....	15
3.2. SL811HS USB CONTROL REGISTERS .....	15
3.3. SL811HS MEMORY MAP.....	16
3.3.1 Control Registers .....	17
3.3.2 Memory Buffer .....	18
3.4. INTERRUPT STATUS REGISTER.....	19
4. SL811HS host software .....	20
4.1. SOFTWARE APPLICATION.....	20
4.1.1 Single Write Operation.....	20
4.1.2 Single Read Operation.....	21
4.1.3 Memory Test.....	21
4.1.4 USB Reset.....	22
4.1.5 CRC5/16 Generation .....	23
4.1.6 Zero Length Packet.....	23
4.1.7 Double Buffer Operation .....	23
4.1.8 Single IN Packet .....	24
4.1.9 Single OUT Packet .....	25
4.1.10 Short Data Packet.....	25
4.1.11 USB Device Detection .....	26
4.1.12 Full/Low Speed Detect.....	26
4.1.13 SOF or EOP Generation .....	28
4.1.14 Suspend State .....	30
4.1.15 Resume Wakeup .....	30
4.1.16 Specific Command Transfer .....	31
4.1.17 USB Transfer (Bulk/ISO/Control/Interrupt) .....	31
4.1.18 Device Enumeration.....	32
5. SL811HS usb transfer .....	33
5.1. CONTROL TRANSFER.....	36

5.1.1	SETUP Transaction .....	37
5.1.2	Control Read.....	37
5.1.3	Control Write .....	39
5.2.	BULK TRANSFER.....	40
5.2.1	BULK Write .....	40
5.2.2	BULK Read .....	41
6.	Error Recovery Management .....	42
6.1.	SL811HS ERROR CONDITIONS.....	42
6.2.	DATA TOGGLE ERROR.....	42
6.3.	BUS TIMEOUT ERROR.....	43
6.4.	BABBLE AND LOSS OF ACTIVITY (LOA).....	43
Figure 1: SL811HS circuit diagram.....		9
Figure 2: SL811HS Host/Slave diagram .....		10
Figure 3: SL811HS Internal Memory Map.....		16
Figure 4: Zero Length Data Packet .....		23
Figure 5: EOP Pulse Width.....		28
Figure 6: Token Phase .....		29
Figure 7: Data Phase.....		29
Figure 8: Handshaking phase.....		29
Table 1: SL811HS and PC address .....		16
Table 2: USB Control Register Memory .....		17
Table 3: SL811HS Control Register Memory Map.....		17
Table 4: DATA0/DATA1 Mapping.....		18
Table 5: Buffers use for configuration and Vendor Specific command .....		18
Table 6: SL811HS Code Bit Definitions.....		18
Table 7: Error Conditions.....		42
Program Sample 1: Single Write Function .....		20
Program Sample 2: Write Buffer Function .....		21
Program Sample 3: Single Read Function .....		21
Program Sample 4: Read Buffer Function .....		21
Program Sample 5: Memory Test.....		21
Program Sample 6: USB Reset Function.....		22
Program Sample 7: Data, Endpoint, and Address .....		23
Program Sample 8: Single IN Packet .....		24
Program Sample 9: Single OUT Packet .....		25
Program Sample 10: Short Data Packet .....		26
Program Sample 11: Speed Detect Function.....		27
Program Sample 12: Hardware EOP Generation .....		29
Program Sample 13: Suspend State.....		30
Program Sample 14: Resume Wakeup.....		30
Program Sample 15: Vendor Command .....		31
Program Sample 16: Vendor Command .....		31
Program Sample 17: USB Control Transfer .....		31
Program Sample 18: Device Enumeration .....		32
Program Sample 19: Device Enumeration .....		32

USB Trace 1: USB Reset .....	23
USB Trace 2: IN Packet .....	24
USB Trace 3: OUT Packet .....	25
USB Trace 4: SOF Packet.....	29
USB Trace 5: EOP Packet.....	30
USB Trace 6: SETUP Transaction .....	37
USB Trace 7: IN Transaction from Device to Host .....	37
USB Trace 8: OUT Transaction from Host to Device .....	39
USB Trace 9: OUT Transaction from Host to Device .....	39
USB Trace 10: Bulk Write.....	40
USB Trace 11: Bulk Read .....	41

## CONVENTIONS

1,2,3,4	Numbers without annotations are decimals.
Dh, 1Fh, 39h	Hexadecimal numbers are followed by an "h".
0101b, 010101b	Binary numbers are followed by a "b".
<i>bRequest, n</i>	Words in <i>italics</i> indicate terms defined by USB Specification or by this Specification.
SL811HS	refers to SL811HS in either 28PLCC or SL811HST - 48LPQFP package.

## DEFINITIONS

USB                      **Universal Serial Bus**

## REFERENCES:

- [Ref 1] SL811HS Specification
- [Ref 2] USB Specification 1.1
- [Ref 3] Human Interface Device support for SL811HS (sl811hs\_hid\_hub.pdf)
- [Ref 4] Host Debugger Document (host\_debugger.pdf)

Please direct any questions about this document to

## REVISION HISTORY

Name and Version	Date Issue	Description	Author/Revise
First Draft	Sept 26, 2000	Created	TBN
Second Draft	10/24/2000		Bernie
Preliminary	02/02/01	Added USB software Tech. support	TBN
Version 1.13	02/06/2001	Version 1.13	KPS
Version 1.16	02/15/2001	Preliminary release	Bernie+TBN+KPS
Version 1.17-1.19	05/17/2001	Add handle USB hub & low speed	TBN
Version 1.21	12/12/2001	Changed name & logos to Cypress	SIK

## 1. INTRODUCTION

### 1.1. Overview

The SL811HS USB Host Controller is a single chip USB embedded host device that can communicate with either full or low speed USB peripherals. The SL811HS can interface to devices such as microprocessors, microcontrollers, DSP's, or to a variety of buses such as ISA, PCMCIA and others. The SL811HS is suitable for use in a variety of embedded systems that require configurable USB host or device features. Typical applications include: Personal Digital Assistants (PDA), Set-top boxes, POS, Medical Test Instruments, Digital Video or Still Cameras, Scanners, Printers, Mobile/Cellular Phones, Game devices, etc.



Host and Slave Application Example



Host Application Example

## 2. SL811HS HOST OR SLAVE MODE

### 2.1. Overview

The SL811HS supports both USB Host and USB Slave modes. These modes are selectable by a single pin that can be permanently connected to ground for Host mode, or left unconnected for Slave mode. Optionally, the Mode Select pin can be driven by a GPIO pin of a host CPU thus allowing software selection of the USB Host/Slave modes. In certain applications, the user may need to support both Host and Slave modes with a single SL811HS controller. The following will describe an application whereby the SL811HS can be utilized to support both modes. A schematic diagram is provided (Figure 1: SL811HS circuit diagram) to illustrate a possible implementation.

### 2.2. Hardware requirements

There is a minimum set of requirements to implement the host/slave functions with a single SL811HS. These are described below in Table 1 below.

#### 2.1.1 External Controller and USB connectors

The application requires an external microcontroller that can provide at least two 3.3V GPIO lines to control the Host/Slave mode pin, and sufficient power to supply to the USB connector when Host mode is enabled.

The USB 1.1 specification requires the use of different USB connectors for Host and Slave ports, and specific termination resistors for each port. The schematic diagram (Figure 2: SL811HS circuit diagram/Figure 2: SL811HS host/slave diagram) illustrates the requirements for each mode.

### 2.3. Power On and Reset Mode

The SL811HS needs to be reset and reconfigured when switched to different modes. The SL811HS has a hardware RESET input that can be used rather than recycling power on/off whenever the mode switch is initiated. For instance, when switching to the Host mode, after the hardware reset, the user sets bit 7 = '1' of Control2 Register (Control2 Register = 0x0F), SL811HS will be in host mode. Please note when both Host and Slave USB connectors are present as shown in the diagram, only one device can be attached at any one time. The following summary of actions has to be accomplished in switching between modes:

Host Mode:

- Pin M/S must set low
- Issue HW reset.
- Set bit-7=1 of t register
- Data+ - switch pull-up 1.5K ohms resistor to disconnect
- Data+ and Data- switch pull-down 15k ohm resistors to ground
- Provide power to pin-1 of USB connector

Slave Mode:

- Pin M/S must set high.
- Issue HW reset.
- Data+ - switch pull-up 1.5K ohm resistor to Vdd.
- Data+ and Data- switch pull-down 15K ohm resistors to disconnect.
- Disconnect power from pin-1 of USB connector.

## 2.4. Switching Logic

The schematic diagrams illustrate a possible implementation using open collector logic devices to switch the pull-up and pull-down resistors, an inverter and a power switch.

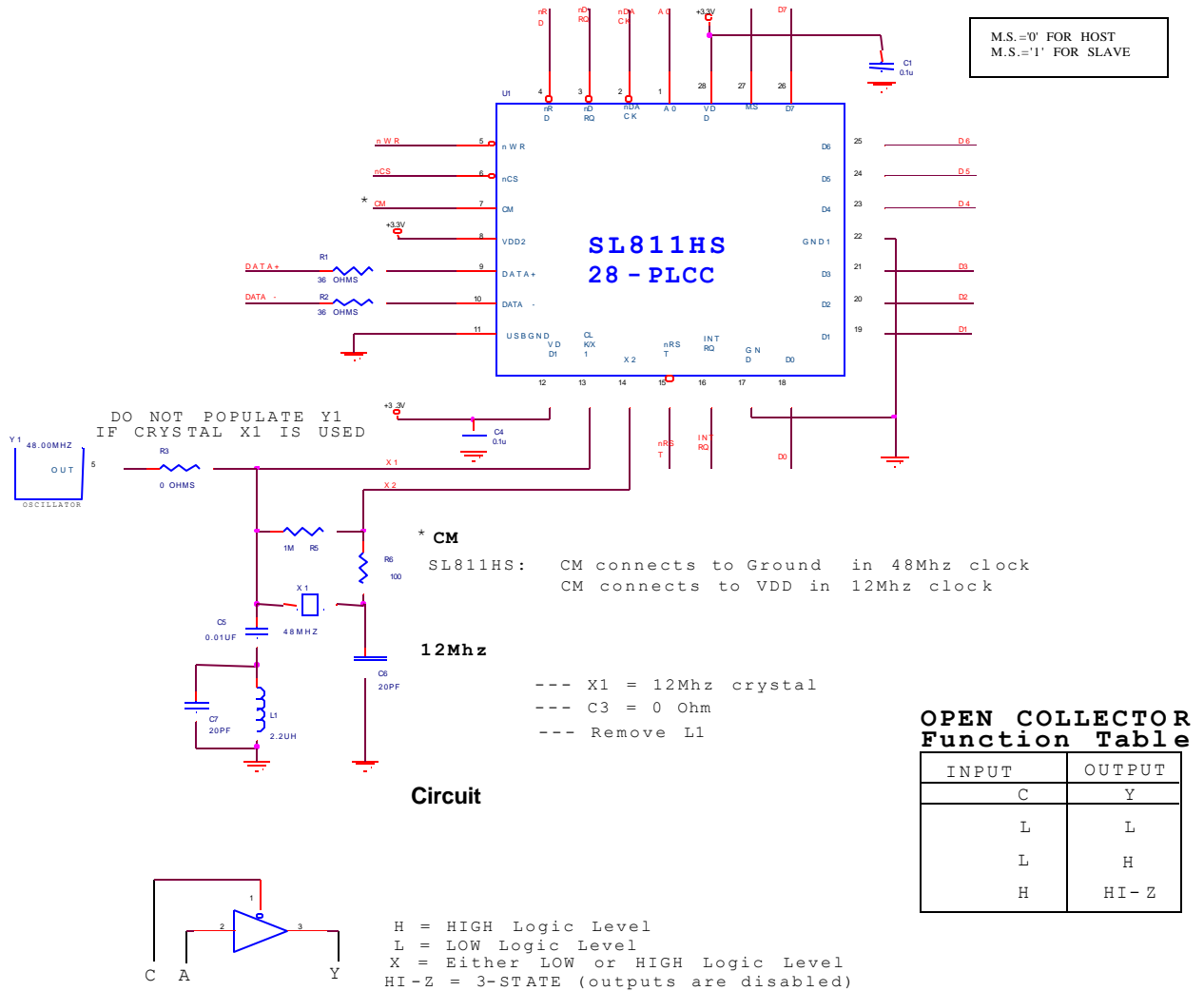


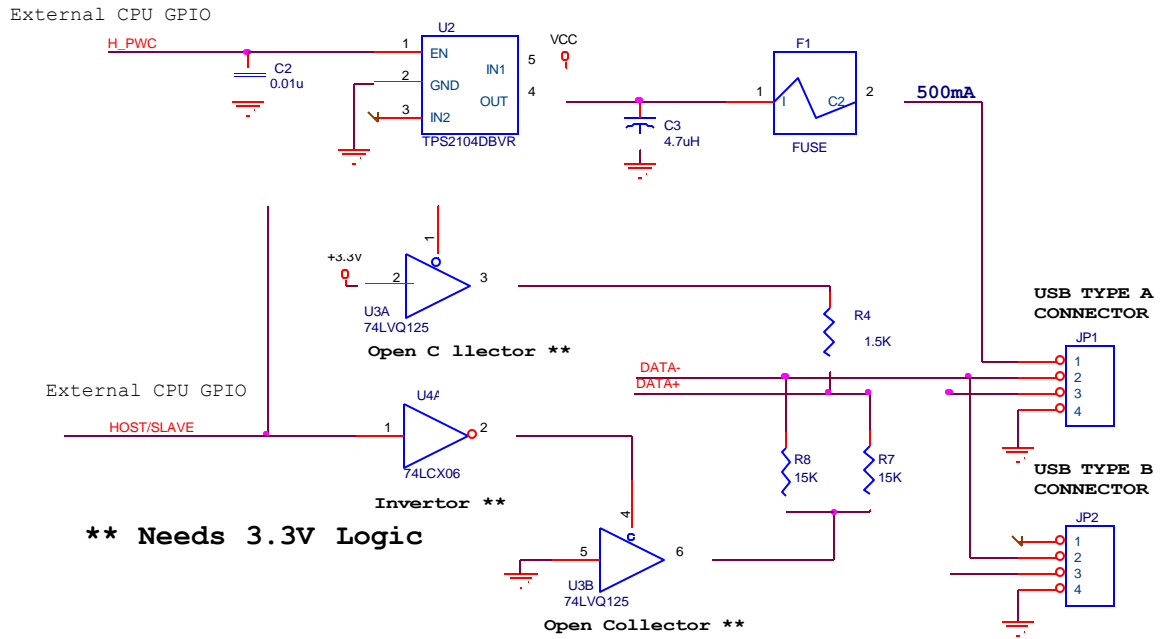
Figure 1: SL811HS circuit diagram



**NOTE:**

**CONNECT EXTERNAL DEVICE TO EITHER JP1 OR JP2.**

**NEVER CONNECT TO BOTH SIMULTANEOUSLY.**



**Figure 2: SL811HS Host/Slave diagram**

## 2.5. Software Initialization

Cypress provides Host and Slave code in development Kit. To switch Host/Slave mode, you need to write an appropriate value to the register 0FH of SL811HS. After writing value to register 0FH, you need to do Initialization.

## 2.5.1 Initialization from Host to Slave

This software initialization is on SL811HS slave mode. This assumes hardware is already configured slave mode.

- Power up
- Config slave mode
  - o Write value "0x00" to register 0FH
- Memory Test
- Slave Initialization:
  - o Reset chip
  - o Disable Interrupt Enable
    - Write value "0x00" to register 06H
  - o Setup USB Address
    - ℳ Write value "0x00" to register 07H
  - o Setup endpoint 0 address starts at 0x40
    - ℳ Write value "0x40" to register 01H
  - o Setup transfer length of endpoint 0
    - ℳ Write value "0x40" to register 12H
  - o Set Arm and direction bit
    - ℳ Write value "0x03" to register 00H

### Endpoint 1 Set A:

- o Setup address Endpoint 1 starts at 0x60
  - ℳ Write value "0x60" to register 11H
- o Setup endpoint 1 transfer length
  - Write value "0x40" to register 12H
- o Set Arm and direction bit
  - ℳ Write value "0x03" to register 10H

### Endpoint 2 Set A and B:

- o Setup Endpoint2A address starts at 0x80
  - ℳ Write value "0x80" to register 21H
- o Setup Endpoint2B address starts at 0xC0
  - Write value "0xC0" to register 29H
- o Setup Endpoint2A transfer length
  - ℳ Write value "0x40" to register 22H
- o Set Arm and direction bit
  - ℳ Write value "0x03" to register 10H
  
- o Interrupt Enable for Endpoint 0, 1, 2, SOF and USB reset
  - Write value "0x67" to register 06H
- o Enable USB Transfer
  - ℳ Write value "0x01" to register 05H
- o Clear Interrupt Status
  - ℳ Write value "0xFF" to register 0DH

## 2.5.2 Initialization from Slave to Host

This software initialization is on SL811HS host mode. This assumes hardware is already configured host mode.

- Power up
- Config host mode
  - o Write value "0xAE" to register 0FH
- Enable power to USB device
- Delay for hardware stable before detect USB device
  - o Delays (25,0); // Delay 25 mili-second
- Memory Test
- Host Initialization:
  - o Hardware reset chip
  - o Interrupt Enable on set USB\_AB, Insert/Remove, and USB Reset
  - o USB Reset, set full speed, and clock 12/48 Mhz mode
    - ✗ Write a value "0x48" to register 05H
  - o Disable USB Transfer and SOF generation
    - ✗ Write a value "0x00" to register 05H
- Full/Low Speed Detection
  - o If bit-7 of Interrupt Status (0DH) equal 0, it is Low speed device.
    - ✗ Write value "0xFF" to register 0EH
    - ✗ Write value "0x0E" to register 0EH
    - ✗ Write value "0x21" to register 05H
  - o If bit- 7 of Interrupt Status (0DH) equal 1, then it is Full speed device.
    - ✗ Write value "0xAE" to register 0EH
    - ✗ Write value "0x0E" to register 0EH
    - ✗ Write value "0x05" to register 05H
  - o Otherwise if there is no power or no device attach clear Interrupt Status
    - ✗ Write value "0xFF" to register 0DH
- Generate SOF to USB device
  - o Write a value "0x50" to register 00H
  - o Write a value "0x00" to register 04H
  - o Write a value "0x01" to register 00H
- Delay for Hardware stable before enumeration
  - o Delays (10,0); // Delay 10 mili-second

## 2.6. M/S pin (pin27/pin40)

It is recommended that M/S pin is “NC”. If you want to set the “Host” or “Slave” mode as power-on-default, you need to make M/S pin be tied to

Mode	M/S pin
Host	GND
Slave	VCC3.3

## 2.7. Pull-up/down registers on USB lines

A 1.5K pull-up resistor is required for “Slave” mode, a 15K pull-down resistors is required for “Host” mode. You will need to enable/disable each registers.

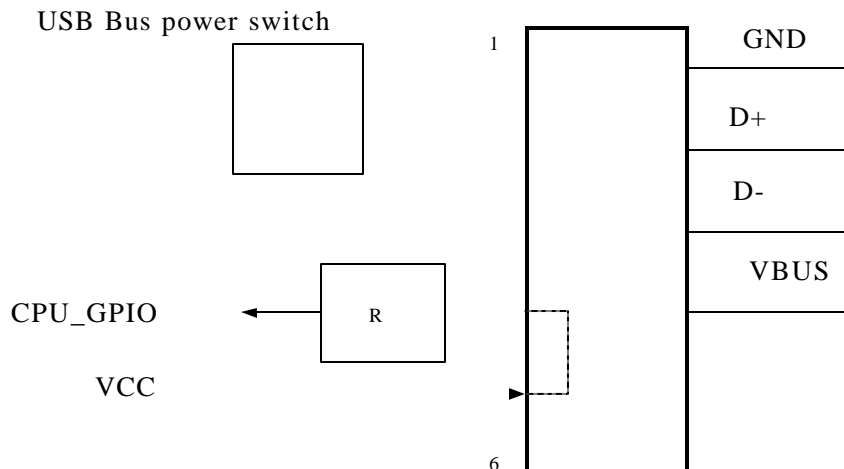
NOTE: See the “SL811HS and SL811HST Application Notes page.8” for more details.

## 2.8. Host/Slave detector

Since the SL811HS does not have a mechanism to know if the inserted device is operating as “Host” or as “Slave”, you need to add a Host/Slave detector. Following are examples of this.

(Example.1) Using 2 different cable with special connectors either “Host” or “Slave”

Connector for Host (pin5 and 6 are inter-connected.)



以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：<https://d.book118.com/826224215043010102>