JEDEC STANDARD

Stress-Test-Driven Qualification of Integrated Circuits

JESD47L

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS

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STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS

(From JEDEC Board Ballot JCB-22-46, formulated under the cognizance of the JC-14.3 Committee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This standard describes a baseline set of acceptance tests for use in qualifying electronic devices as new products, a product family, or as products in a process which is being changed.

These tests are capable of stimulating and precipitating semiconductor device and packaging failure modes on free-standing devices not soldered to a printed wired board (PWB), or the like (base device reliability). The objective is to precipitate failures in an accelerated manner compared to use conditions. Failure Rate projections usually require larger sample sizes than are called out in qualification testing. For guidance on projecting failure rates, refer to JESD85 Methods for Calculating Failure Rates in Units of FITs.

This qualification standard is aimed at a generic qualification for a range of use conditions, but

- may not be applicable at extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments
- does not cover devices assembled onto a PWB, or the like, which may affect the device reliability under assembled state. This is addressed in JEP150 and e.g., typically applies to TC on WLCSP devices

Additional qualification testing tailored to meet specific requirements such as solder joint interconnect reliability can be developed by applying JESD94.

This set of tests should not be used indiscriminately. Each qualification project should be examined for:

a) Any potential new and unique failure mechanisms.

b) Any situations where these tests/conditions may induce invalid or overstress failures.

If it is known or suspected that failures either are due to new mechanisms or are uniquely induced by the severity of the test conditions, then the application of the test condition as stated is not recommended. Alternatively, new mechanisms or uniquely problematic stress levels should be addressed by building an understanding of the mechanism and its behavior with respect to accelerated stress conditions (Ref. JESD91, ‰Method for Developing Acceleration Models for Electronic Component Failure Mechanisms^^ and JESD94, "Application Specific Qualification using Knowledge Based Test Methodology„)·

Consideration of PC board assembly-level effects may also be necessary. For guidance on this, refer to JEPl 50, Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components.

This document does not relieve the supplier of the responsibility to assure that a product meets the complete set of its requirements.

2 Normative References

The revision of the referenced documents shall be that which is in effect on the date of the qualification plan.

2.1 Military

MIL-STD-883, *Test Methods and Procedures for Microelectronics.*

MIL-PRF 38535, *General Specificationfor Integrated Circuit Manufacturing.*

2.2 Industrial

UL94, *Testsfor Flammability of Plastic Materials for Parts in Devices and Appliances.*

ASTM D2863, *Flammability of Plastic Using the Oxygen Index Method.*

IEC Publication 695, *Fire Hazard Testing.*

J-STD-020, Joint IPC/JEDEC Standard, *MoistureZReflow Sensitivity Classification for Non-hermetic Solid State Surface-Mount Devices.*

JP-OOl, *Foundry Process Qualification Guidelines (Wafer Fabrication Manufacturing Sites).*

JS-OO1, *Joint JEDEC/ESDA Standard for Electrical Discharge Sensitivity Test - Human BodyModel (HBM) -Component Level*

JS-002, *ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Device Level*

J-STD-002, *Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires*

JESD22 Series, *Reliability Test Methods for Packaged Devices*

JESD46, *Guidelines for User Notification of ProductZprocess Changes by Semiconductor Suppliers.*

JESD69, *Information Requirements for the Qualification of Silicon Devices.*

JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.*

JESD78, *IC Latch-Up Test.*

JESD85, *Methods for Calculating Failure Rates in Units of FITs.*

JESD86, *Electrical Parameters Assessment.*

JESD91, *Methods for Developing Acceleration Modelsfor Electronic Component Failure Mechanisms.*

JESD94, *Application Specific Qualification using Knowledge Based Test Methodology.*

JEP122, *Failure Mechanisms and Models for Semiconductor Devices.*

JEP143, *Solid State Reliability Assessment Qualification Methodologies.*

JEPl 50, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated WithAssembled Solid State Surface-Mount Components.*

JEP156, *Chip-Package interaction Understanding, Identification and Evaluation.*

JESD201, *Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes.*

3 Gelleral ReqiIiremelItS

3.1 Objective

The objective of this procedure is to ensure that the device to be qualified meets a generally accepted set of stress test driven qualification requirements. Qualification is aimed at devices predominantly used in commercial or industrial operating environments. For other applications, such as automotive, avionics, medical, etc., adjustments to these requirements may be necessary per supplier and customer agreements.

3.2 Qualification Family

While this specification may be used to qualify an individual device, it is designed to also qualify a family of similar devices utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs. Interactive effects of the silicon and package per JEP156 shall be considered in applying family designations.

3.3 Lot Requirements

Test samples shall comprise representative samples from the qualification family. Manufacturing variability and its impact on reliability shall be assessed. Where applicable, the test samples will be composed of approximately equal numbers from at least three (3) non-consecutive lots. Other appropriate means may be used to evaluate manufacturing variability. Sample size and pass/fail requirements are listed in Table 1, Table 2, Table 3, Table 4, Table 5,and Table 6 providing guidance on translating pass/fail requirements to larger sample sizes.

Generic data and larger sample sizes may be employed based upon a Chi Squared distribution using a total percent defective at a 90% confidence limit for the total required lot and sample size. ELFR requirements shall be assessed at a 60% confidence level as shown in Table 4. If a single unique and expensive device is to be qualified, a reduced sample size qualification may be performed using 1/3 the sample size listed in the qualification tables.

3.4 Production Requirements

All test samples shall be fabricated and assembled in the same production site and with the same production process for which the device and qualification family will be manufactured in production. Samples need to be processed through the full production process including burn-in, handling, test, and screening.

3.5 Reusability of Test Samples

Devices that have been used for non-destructive qualification tests may be used to populate other qualification tests. Devices that have been used in destructive qualification tests may not be used in subsequent qualification stresses except for engineering analysis. Non-destructive qualification tests are: Early Life Failure Rate, Electrical Parameters Assessment, External Visual, System Soft Error, and Physical Dimensions.

3.6 Definition of Electrical Test Failure After Stressing

Post-stress electrical failures are defined as those devices not meeting the individual device specification or other criteria specific to the environmental stress. If the cause of failure is due to causes unrelated to the test conditions, the failure shall be discounted.

3.7 Required Stress Tests for Qualification

Table 2, Table 5, and Table 6 list the qualification requirements for new devices. Table 5 and Table 6 are differentiated by package type, but these are not exclusively packaging tests. As outlined in JEP156, interactive effects of the packaging on the silicon also drive the need for tests in Table 5 and Table 6. Power supply voltage for biased reliability stresses should be V_{cc} max or Vdd max as defined in the device datasheet as the maximum specified power supply operating voltage, usually the maximum power supply voltage is 5% to 10% higher than the nominal voltage. Some tests such as HTOL may allow for higher voltages to gain additional acceleration of stress time. JEP122 can provide guidance for accelerating common failure mechanisms.

Table 7 lists the stresses that should be considered for a qualification family or category of change. Interactive effects from the unchanged aspects of both the silicon and packaging must be assessed.

3.8 Pass/Fail Criteria

Passing all appropriate qualification tests specified in Table 2, Table 5, and Table 6, either by performing the test, showing equivalent data with a larger sample size, or demonstrating acceptable generic data (using an equivalent total percent defective at a 90% confidence limit for the total required lot and sample size), qualifies the device per this document. When submitting test data from generic products or larger sample sizes to satisfy the Table 2, Table 5, and Table 6 qualification requirements of this document, the number of samples and the total number of defective devices occurring during those tests must satisfy 90% confidence level of a Poisson exponential binomial distribution, as defined in MIL-PRF 38535. MIL-PRF 38535 is available for free from:
http: 〃 WWW.dscc.dla.mil/ProgramS/MilSpec/IiStdOCS.asp?BaSiCDOC=MIL-PRF-38535.

The minimum number or samples for a given defect level can be approximated by the formula:

$$N \geq 0.5\ [\chi^2\ (2C+2,\ 0.1)]\ [1/LTPD - 0.5] + C$$

where C = accept #, N = Minimum Sample Size, χ^2 is the Chi Squared distribution value for a 90% CL, and LTPD is the desired 90% confidence defect level. Table 1 is based upon this formula, but in some cases the sample sizes are slightly smaller than MIL-PRF-38535.

3.9 Pass/Fail Criteria (cont·d)

Table 1 — Zero DefeCt SamPIe SiZeS for StreSS TeStS

Zero Defect Sampling should be set based on defect type, process maturity and specific application

Samples per batch	No. of batches	Total Sample	Confidence Level (defect rate) 40%	50%	60%	75%	90%
77	3	231	<0.2%	<0.3%	≤0.4%	<0.6%	**≤ 1.0% ***
45	3	135	<0.4%	<0.5%	<0.7%	**≤ 1.0% ***	< 1.7%
30	3	90	<0.6%	<0.8%	**≤ 1.0% ***	≤ 1.5%	<2.6%
25	3	75	<0.7%	**≤ 0.9% ***	≤ 1.2%	≤1.8%	<3.1%
15	3	45	**≤1.1% ***	≤1.5%	<2.0%	≤3.1%	<5.1%

* Suggested sampling per confidence level.

Specific sample plan can be established according to a desired defect rate, and consider the defect type, process maturity and understanding of device application. Agreement between suppliers and customers is recommended.

The confidence levels in Table 1 reflect a zero defect sampling response. For instance, reaching O defects for 231 samples would demonstrate <1.0% defect rate at 90% confidence level. Conversely, for 0 defects at 90 samples, ≤1.0% defect rate would only carry at 60% confidence.

However, other equivalent defect rates and confidence levels can also be considered using larger sample sizes and non-zero fail counts in accordance with the same non-parametric binomial probability. Refer to Annex B for different sampling plan.

4 Qualification and Requalifications

4.1 Qualification of a New Device

New or redesigned products (die revisions) manufactured in a currently qualified qualification family may be qualified using one (1) wafer/assembly lot. Electrical parameter assessment to accompany each test should be conducted.

4.2 Requalificatioii of a Changed Device

Requalification of a device will be required when the supplier makes a change to the product and/or process that could potentially impact the form, fit, function, quality and/or reliability of the device. A list of changes that may require requalification is shown in clause 6.1.

4.2.1 Process Change Notification

Supplier should follow the guidelines of J-STD-046 "Guidelines for User Notification of Product/Process Changes by Semiconductor Suppliers" for product/process notification changes to consider whether requalification of a device is warranted.

4.2.2 Changes Requiring Requalification

All product/process changes should be evaluated against the guidelines listed in Table 7.

4.2.3 Criteria for Passing Requalificatioii

Table 7 lists qualification plan guidelines for performing the appropriate Table 2, Table 5, and Table 6 stresses. Failed devices should be analyzed for root cause and correction; only a representative sample needs to be analyzed. Acceptable resolution of root cause and successful demonstration of corrective and preventive actions will constitute successful requalification of the device(s) affected by the change. The part and/or the qualification family can be qualified as long as containment of the problem is demonstrated until corrective and preventive actions are in place.

5 QUaHfiCatioiI TeStS

5.1 General Tests

Test details are given in Table 2, Table 5, and Table 6. Not all tests apply to all devices. Table 2 tests generally apply to design and fabrication process changes. Table 5 tests are for non-hermetic packaged devices, and Table 6 is for hermetic packaged devices. Table 4 lists the pass/fail requirements for common infant mortality levels. Table 7 gives guidance as to which tests are required for a given process change. Some of the data required may be substituted by generic process or package data.

5.2 Device Specific Tests

The following tests must be performed on the specific device to be qualified for all hermetic and plastic packages. Passing or failing these tests qualifies or disqualifies only the device under qualification and not the associated qualification family:

1) Electrostatic Discharge (ESD) - All products. See Table 2.
2) Latch-up (LU) - Required for CMOS, BiCMOS, and Bipolar technologies. See Table 2.
3) Electrical Parameters Assessment - The supplier shall be capable of demonstrating, over the application temperature range, that the part is capable of meeting parametric limits in the individual device specification or data sheet.

5.3 Wearout Reliability Tests

Qualification family testing for the failure mechanisms listed below must be available upon request when a new wafer fabrication technology or a material relevant to the appropriate wearout failure mechanism is to be qualified. JPOOl lists requirements for Fabrication Process Qualification. JEP122 explains how to project wearout lifetime for these failure mechanisms. The following mechanisms need to be considered, but there may be other mechanisms to consider based upon technology details.

- Electromigration; EM
- Time-Dependent Dielectric Breakdown; TDDB or Gate Oxide Integrity Test such as Charge to Breakdown.
- Hot Carrier Injection; HCI
- Bias Temperature Instability; BTI
- Stress Migration; SM, may be performed on an actual product.

5.4 Wearout Reliability Tests (cont'd)

The data, test method, calculations, and internal criteria need not be demonstrated or performed on the qualification of every new device.

5.5 FlammabilityZOxygen Index

Certificates of compliance to UL94-0 or ASTM D2863 must be available upon request.

5.6 Device Qualification Requirements

Table 2 ——Device QualificatioiiTests

Stress	Ref.	Abbv.	Conditions	Requirements	
				# Lots / SS per lot	Duration /Accept
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	Tj ≥125°C $V_{CC} \geq V_{CC}$ max	3 Lots / 77 units	1000 hrs / 0 Fail
Early Life Failure Rate	JESD22-A108, JESD74	ELFR	Tj≥ 125°C $V_{CC} \geq V_{CC}$ max	See ELFR Table	48 ≤ t≤ 168 hrs
Low Temperature Operating Life	JESD22-A108	LTOL	Tj ≤ 50°C $V_{CC} \geq V_{CC}$ max	1 Lot / 32 units	1000 hrs / 0 Fail
High Temperature Storage Life	JESD22-A103	HTSL	T_A ≥150°C	3 Lots / 25 units	1000 hrs / 0 Fail
Latch-Up	JESD78	LU	Class I or CIaSS II	1 Lot / 3 units	OFail
Electrical Parameter Assessment	JESD86	ED	Datasheet	3 Lots /10 units	T_A per datasheet
Human Body Model ESD	JS-OOl	ESD-HBM	$T_A = 25^0C$	3 units	Classification
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25^oC$	3 units	Classification
Accelerated Soft Error Testing **OR** System Soft Error Testing	JESD89-2 and JESD89-3 OR JESD89-1	ASER SSER	$T_A = 25^0C$	3 units **OR** Minimum of 1E+O6 Device Hrs or 10 fails.	Classification

The Abbreviations column in Table 2 is elaborated upon here:

a) **HTOL -** The duration listed here is generally acceptable to qualify for the given Application Level. However, it does not necessarily imply the demonstration of the lifetime requirement for a particular use condition. It depends on failure mechanisms and application environments. For example, with apparent activation energy of 0.7 eV, 125°C stress temperature and 55°C use temperature, the acceleration factor (Arrhenius equation) is 78.6. This means IOOO hour stress duration is equivalent to 9 years of use. This might be shorter than the application requirement. The equivalent life can be even lower for products or technologies where activation energies are less (e.g., 0.4 eV yields an acceleration factor of ~12 or 1.4 years of equivalent life). In order to assure adequate lifetime requirement, it would be necessary to include Wafer Level Reliability Test information. Wafer Level Reliability can provide information about long term or intrinsic reliability of specific die-level wearout mechanisms, the onset to failure time and design rule (e.g., maximum current density).

5.5 Device Qualification Requirements (cont'd)

For many failure mechanisms, such as dielectric breakdown, elevated voltage will provide additional acceleration and can be used to increase effective device hours or achieve an equivalent life point with a shorter stress duration. Refer to JEP122 for voltage acceleration models. Non-volatile memory devices must be tested for proper operation after HTOL, but testing for data retention is optional (see Table 3 for non-volatile memory data retention tests).

b) ELFR - Several methods can be used to calculate the Early Life Failure Rate (ref. JESD74). The objective of ELFR is to measure the failure rate in the first several months or year of operation. Knowledge of the life distribution is generally required to accurately predict ELFR. Equivalently, Table 4 can be used to determine sample sizes to satisfy a particular FPM (cumulative failures) target. Voltage and temperature acceleration may be used to further accelerate effective unit hours. Non-volatile memory devices must be tested for proper operation after ELFR, but testing for data retention is optional (see Table 3 for non-volatile memory data retention tests).

c) **LTOL -** This requirement is aimed at Hot Carrier Degradation and may be satisfied by appropriate wafer level data as specified in JPOOl. This test is particularly useful when the wafer level data cannot demonstrate adequate life. This test should be run at the maximum frequency of the device with speed parameters data logged. Non-volatile memory devices must be tested for proper operation after LTOL, but testing for data retention is optional (see Table 3 for non-volatile memory data retention tests).

d) **HTSL -** High temperature storage may be accelerated by utilizing a higher temperature; however care must be taken that failure mechanisms are not introduced such as Kirkendall Voiding occurring at very high a temperature or suppressing failure mechanisms such as stress migration at temperatures above 180°C. Alternatively, this test may be performed at the wafer level if packaged device reliability has been addressed with generic data. Non-volatile memory devices must be tested for proper operation after HTSL, but testing for data retention is optional (see Table 3 for non-volatile memory data retention tests).

e) **LU -** Verify V_{cc} overvoltage and I/O trigger current resistance to latch-up per JESD78.

f) **ED –** This study is to be performed on key device parameters; it is not aimed at all datasheet parameters.

g) **ESD-HBM -** Classification of Human body Model ESD sensitivity.

h) **ESD-CDM -** Classification of Charge Device model ESD sensitivity.

i) **ASER -** Accelerated alpha particle and beam soft error testing may be utilized together to project the field soft error rate. For parts without B^{10} in the process, the only beam soft error testing required is high energy neutron or proton soft error testing; thermal neutron soft error beam testing is not required for such parts. This test is required for devices with a significant portion of the circuit utilizing volatile memory elements or latches. Generic data taken on products or test devices with similar memory elements or latches and equivalent critical charge may be substituted.

j) **SSER –** System soft error testing requires enough device hours to be accumulated to produce 10 failures or at least 1E6 device hours must be accumulated. High altitude testing may be used to accelerate this stress. This test may be utilized in lieu of or in addition to accelerated soft error testing. Generic data taken on products or test devices with similar memory elements or latches and equivalent critical charge may be substituted.

k)