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1 System Overview

1.1 General Description

This scope of document is to provide a specification of XR819 Wireless LAN SoC, that will be used by the system/design/development teams to detail the design requirements.

XR819 is a fully integrated 2.4G WLAN SoC to support 802.11 b/g/n. It is optimized for mobile applications such as PDAs and portable media players. The low power consumption and intelligent host off loading of beacon as well as the packet processing ensure better battery life. High sensitivity and transmitting power ensure long distance and robust connection. Highest level of integration allows very compact and cost effective reference designs delivering fast time-to-market for new WLAN enabled products. And small 5x5mm QFN package is suitable for very compact design.

1.2 Features

- Compatible with IEEE 802.11 b/g/n standard
- Clocks
  - – XTAL or external reference clock input from 13~52MHz
  - – Internal or external Low power clock at 32.768 kHz
- On-chip auto calibrations
- Intelligent adaptive power control for
  - – Saving power consumption
  - – Tolerating VSWR variation to maintain EVM performance
- WLAN solution with fully integrated
  - – High power PA
  - – TR switch
  - – Internal impedance matching network
  - – OFDM/CCK PHY processor
  - – SDIO 2.0 host interface
- Support for 6 Mbps to 65 Mbps OFDM
  - –11 Mbps and 5.5 Mbps CCK and legacy
  - – 2 Mbps and 1 Mbps DSSS data rates
- WiFi Direct support with concurrent operation
- Supports MAC enhancements including
  - – 802.11d - Regulatory domain operation
  - – 802.11e - QoS including WMM
  - – 802.11h – Transmit power control dynamic and frequency selection
  - – 802.11i - Security including WPA2 and WAPI compliance

– 802.11r - Roaming

– 802.11w - Management frame protection

1.3 Applications

- Tablet PC applications
- Portable media player(PMP) applications
- Portable gaming device(PGD) applications
- Smart internet TV box applications
- Internet of Thing (IOT)

1.4 Block Diagram

Top level block diagram of XR819 is shown in Figure 1-1.

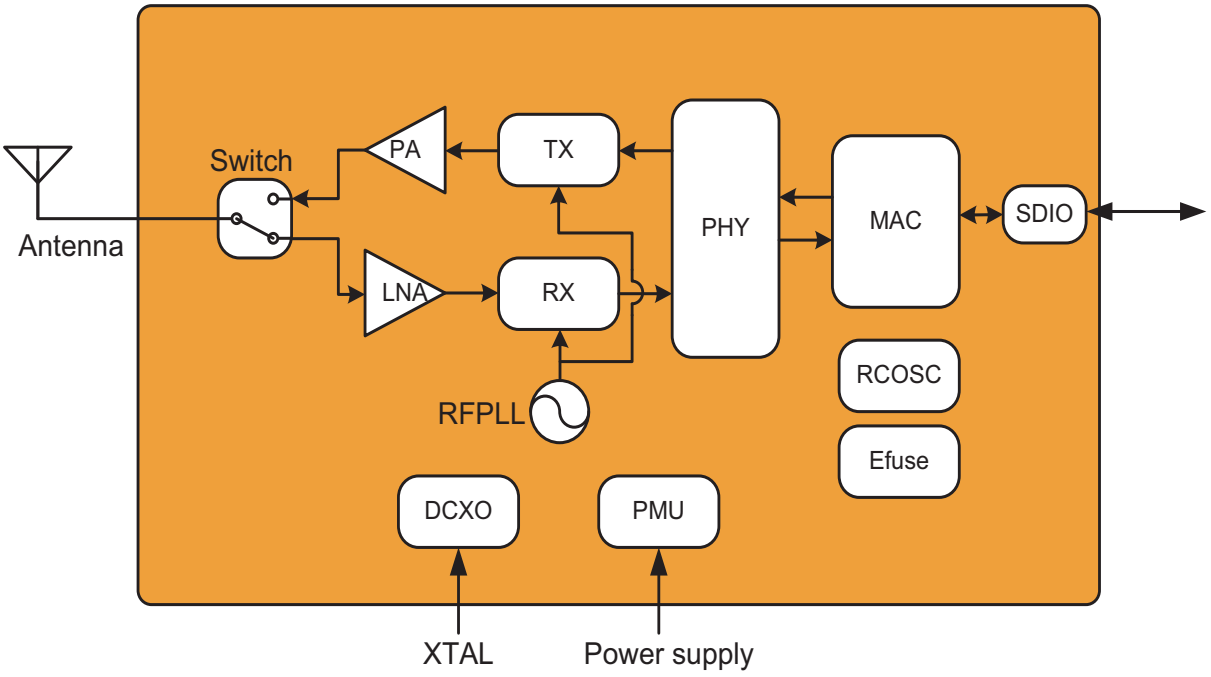

Figure 1-1 XR819 Block Diagram

The WLAN subsystem includes a single-band 2.4G RF transceiver (RX and TX), PA and LNA including RF switch, RFPLL, an OFDM/CCK PHY processor and PMU, that keep data communications with host using SDIO 2.0. This application has industry leading low cost BOM to simplify product development.

2 Pin Description

2.1 Pin Assignment

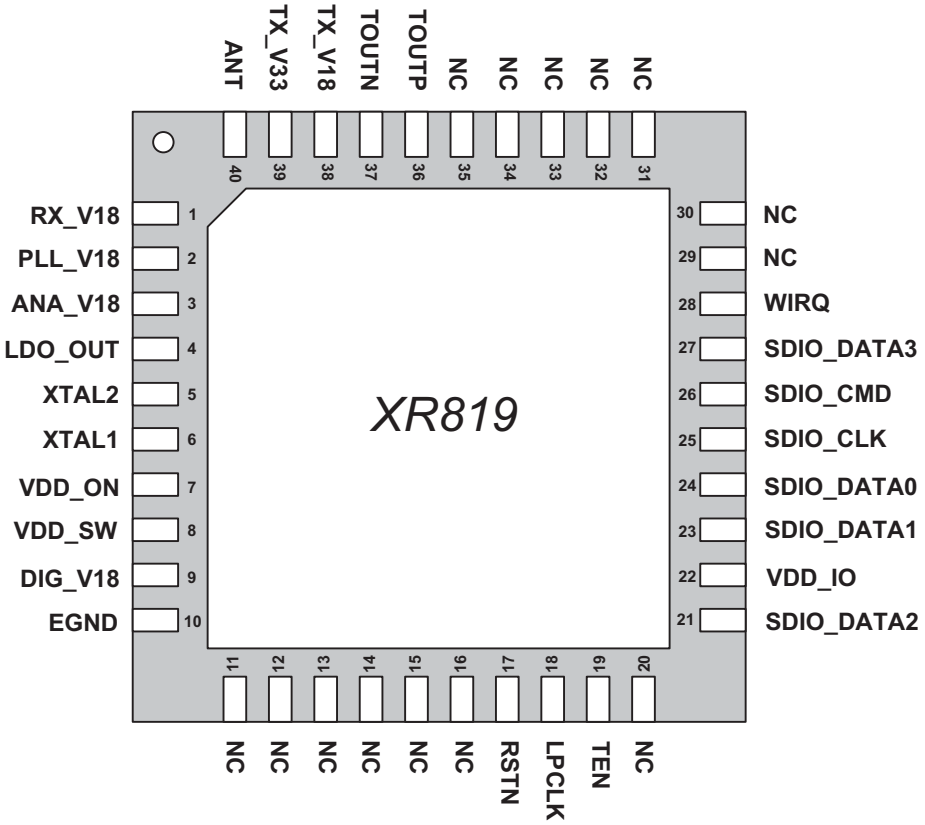

Figure 2-1 Pin Assignment

2.2 Pin List

The following signal type codes are used in the table:

I: Input

O: Output

I/O: for Input/Output

P: Power pin

Table 2-1 Pin List

Name	Pin	Type	Description
Analog			

