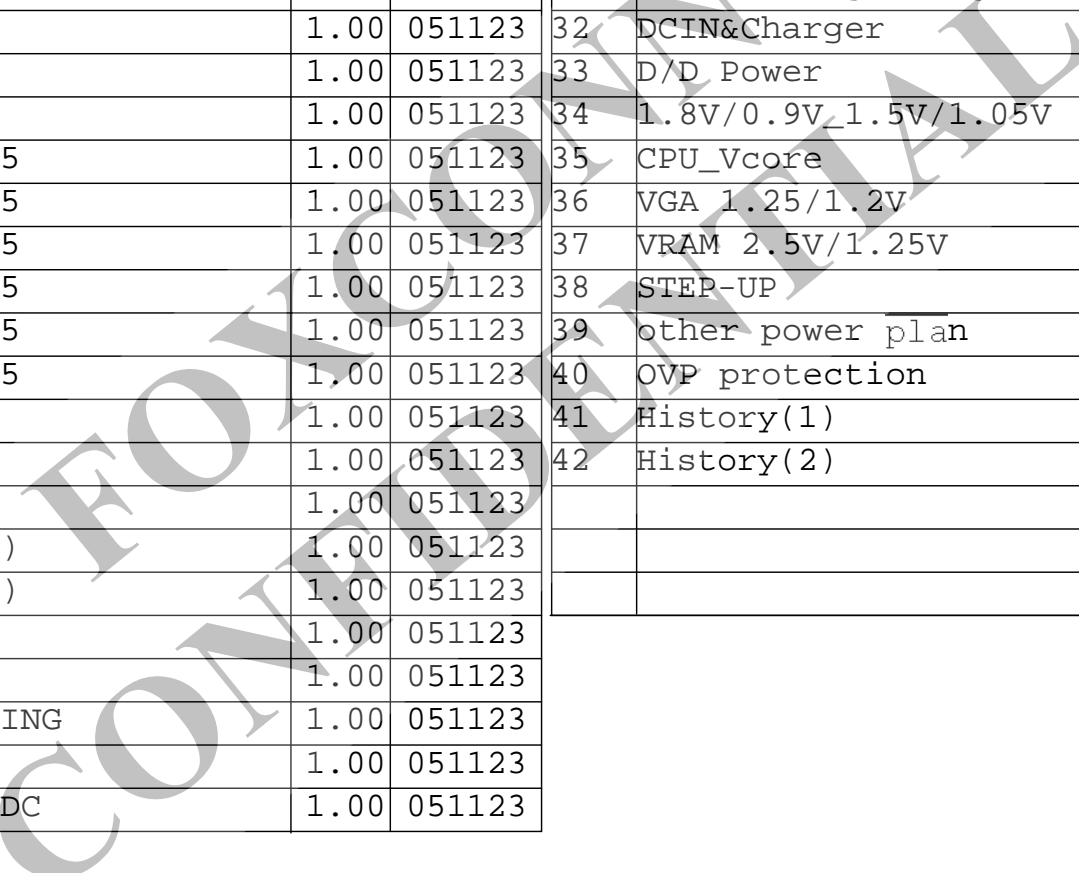


**Schematics Page Index (Title / Revision / Change Date)**

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07	Alviso (VGA,DMI) 2/5	1.00	051123	32	DCIN&Charger	1.00	051123
08	Alviso (DDR) 3/5	1.00	051123	33	D/D Power	1.00	051123
09	Alviso (POWER) 4/5	1.00	051123	34	1.8V/0.9V_1.5V/1.05V	1.00	051123
10	Alviso (VSS,NCTF) 5/5	1.00	051123	35	CPU_Vcore	1.00	051123
11	VGA(nVIDIA NV44M) 1/5	1.00	051123	36	VGA 1.25V/1.2V	1.00	051123
12	VGA(nVIDIA NV44M) 2/5	1.00	051123	37	VRAM 2.5V/1.25V	1.00	051123
13	VGA(nVIDIA NV44M) 3/5	1.00	051123	38	STEP-UP	1.00	051123
14	VGA(nVIDIA NV44M) 4/5	1.00	051123	39	other power plan	1.00	051123
15	VGA(nVIDIA NV44M) 5/5	1.00	051123	40	OVP protection	1.00	051123
16	NV44M(DDR F_A B_1)	1.00	051123	41	History(1)	1.00	051123
17	DDR(II)SO-DIMM	1.00	051123	42	History(2)	1.00	051123
18	DDR(II)Termination	1.00	051123				
19	ICH6-M( CPU,PCI,IDE )	1.00	051123				
20	ICH6-M( USB,HUB,LPC )	1.00	051123				
21	ICH6-M( POWER&GND )	1.00	051123				
22	IDE (HDD&CD_ROM)	1.00	051123				
23	USB2.0/OIDE/FAN/DOCKING	1.00	051123				
24	PCI7420B(PCMCIA)	1.00	051123				
25	PCI7420B(iLink,MS)/MDC	1.00	051123				



P. Leader	Check by	Design by

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CPBG - R&D Division

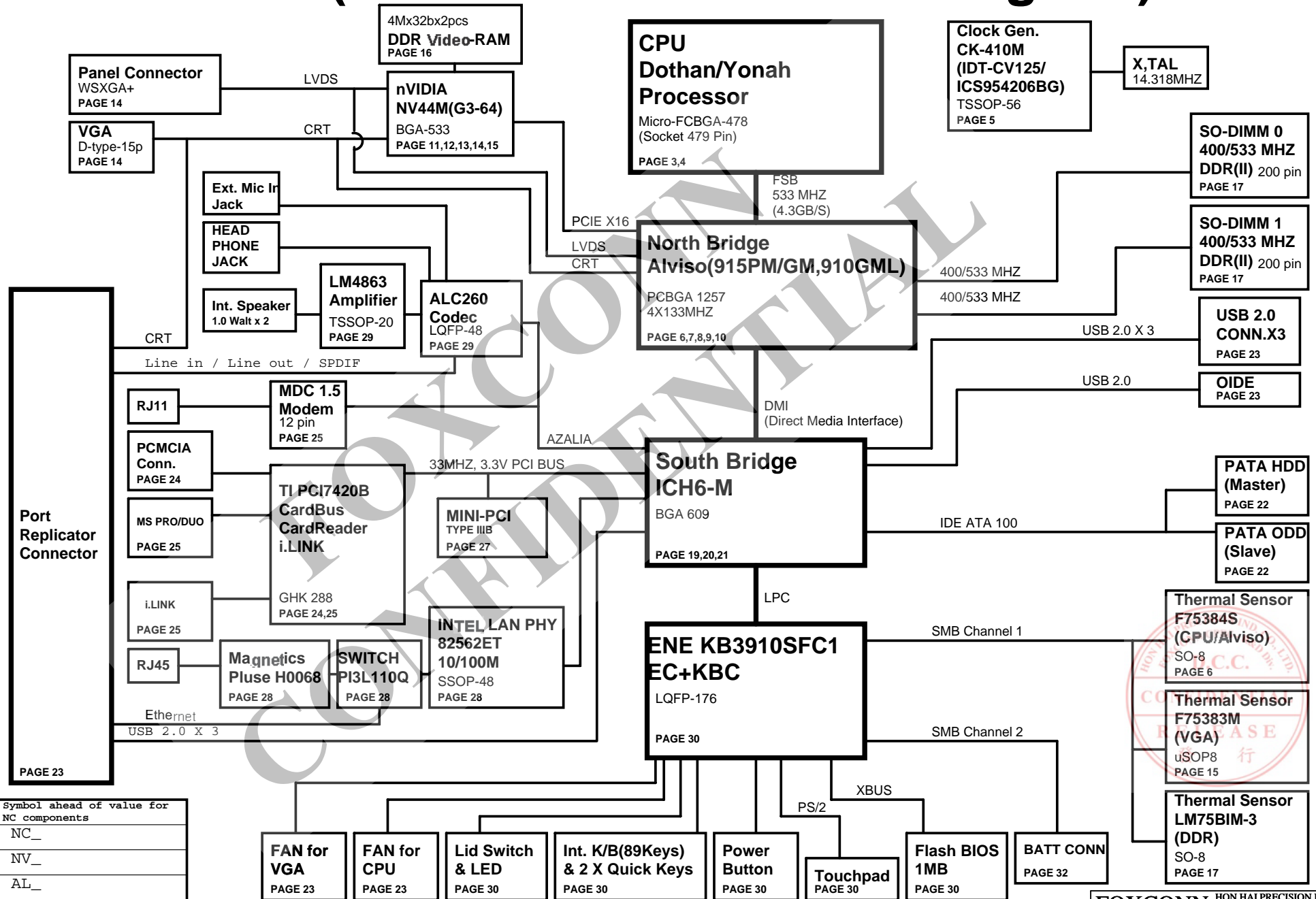
Title: **Index Page**

Size: A3 Document Number: MS04-1-01 Rev: 1.00

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<b>Project Code &amp; Schematics Subject:</b> MS04 M/B-FUBAI	<b>PCB P/N:</b> 1P-005B100-8012
<b>Project Code &amp; Schematics Subject:</b> MS04 M/B-HANNSTAR	<b>PCB P/N:</b> 1P-005B500-8012
<b>Project Code &amp; Schematics Subject:</b> MS04 M/B-NAN YA	<b>PCB P/N:</b> 1P-005B200-8012

# MS04(915PM/GM+Gfx Block Diagram)



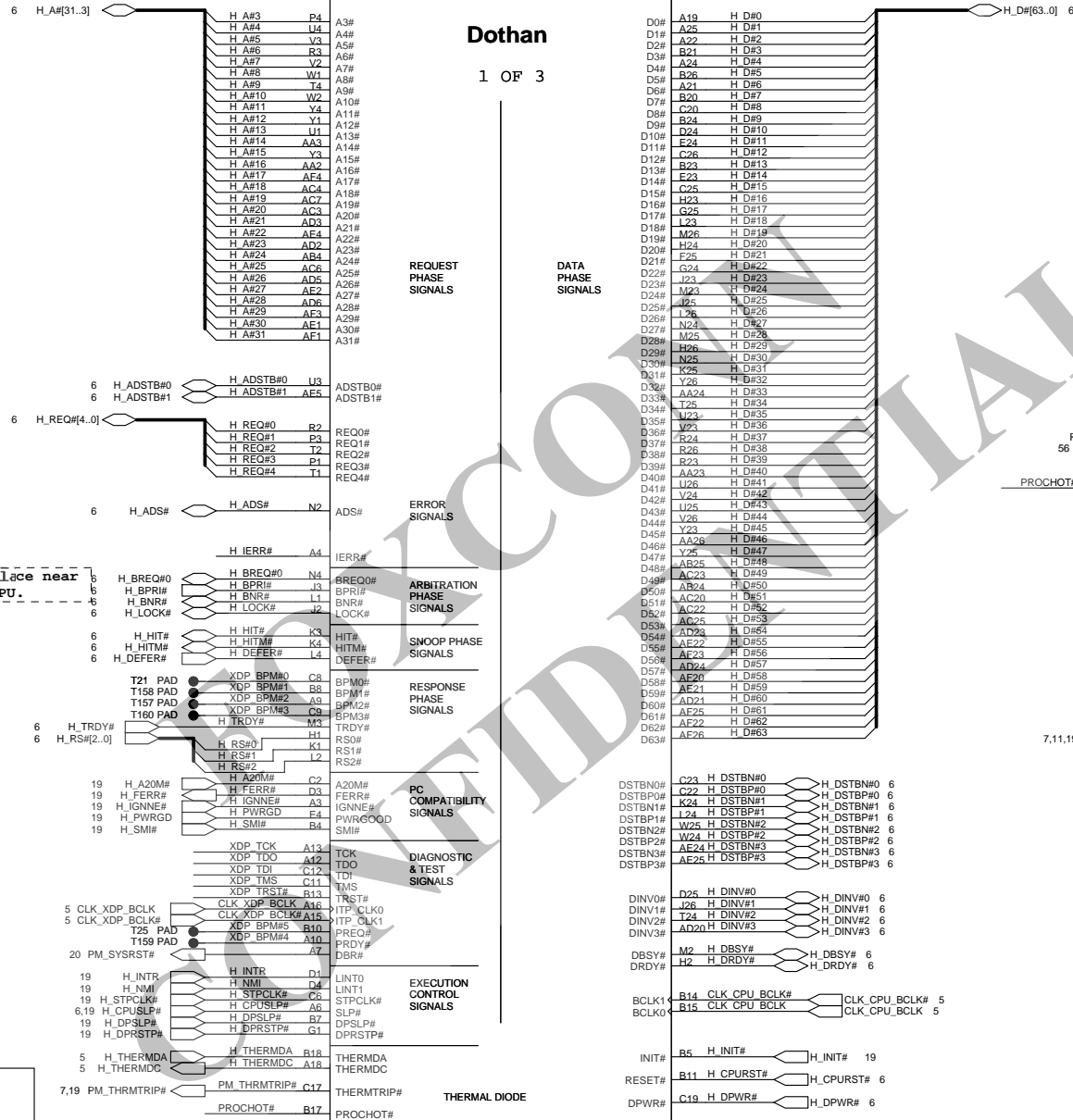
	Symbol ahead of value for NC components
ALL	NC_
915PM + NV44M	NV_
915GM or 910GML	AL_
910GML	LNC_
915PM + NV44M or 915GM	HMNC_

BOM configuration

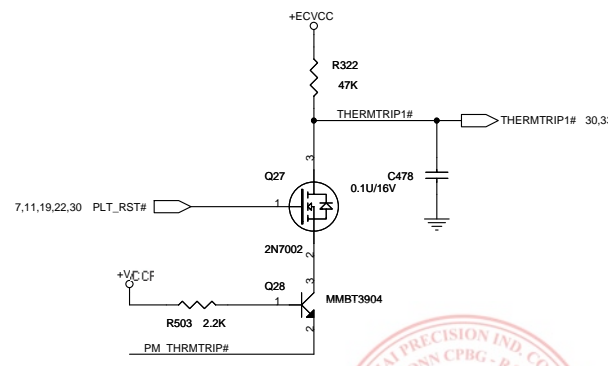
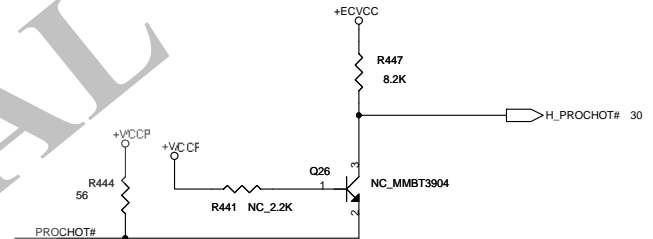
Dothan

1 OF 3

U30A

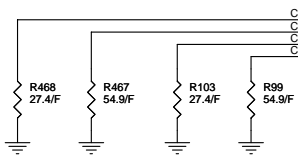


Dothan Processor

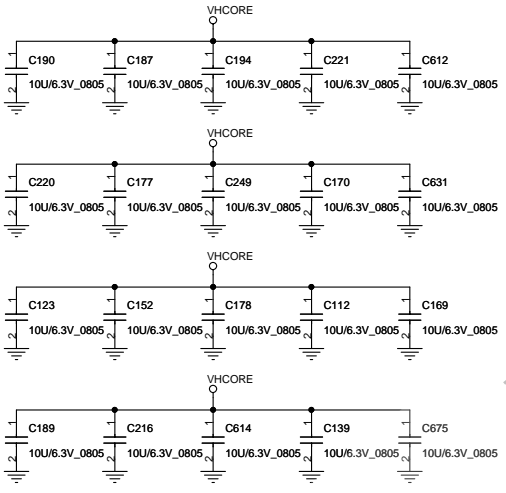
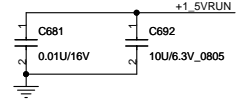
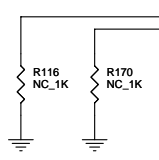


PM\_THRMTRIP# should connect to ICH6-M and ALVISO without T-ing (No stub)

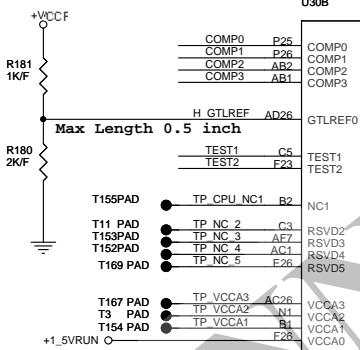
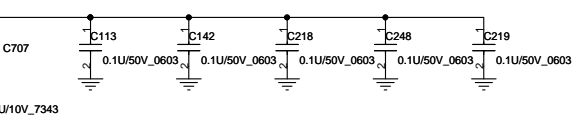
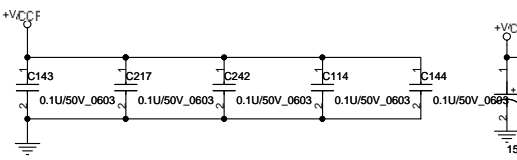




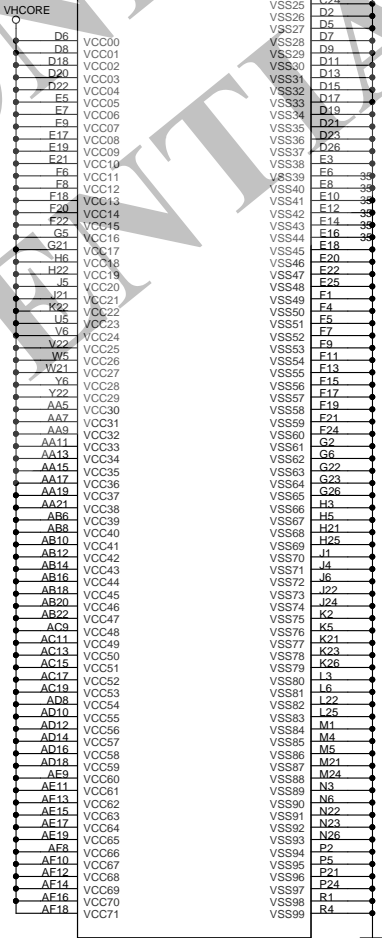
Place pull-down resistors within 0.5" of COMP pins



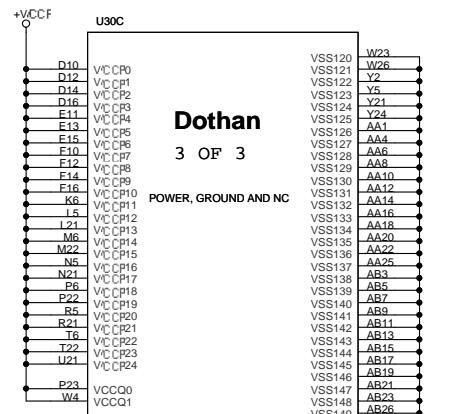
Total caps = 2633 uF  
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



Dothan  
2 OF 3

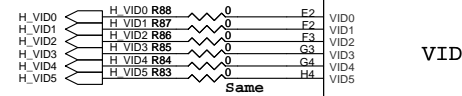


Dothan Processor

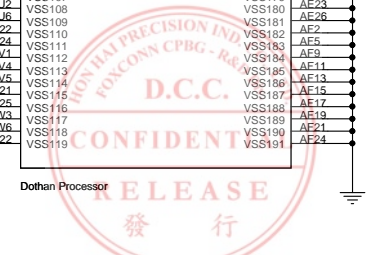
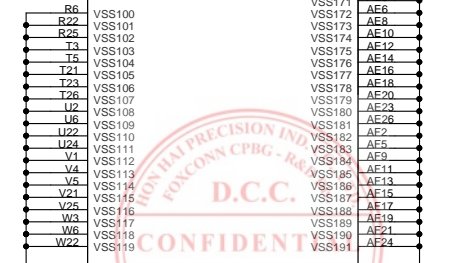
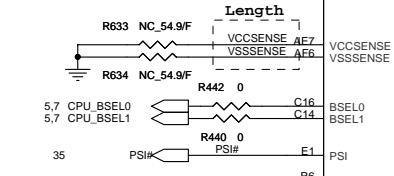


Dothan  
3 OF 3

POWER, GROUND AND NC



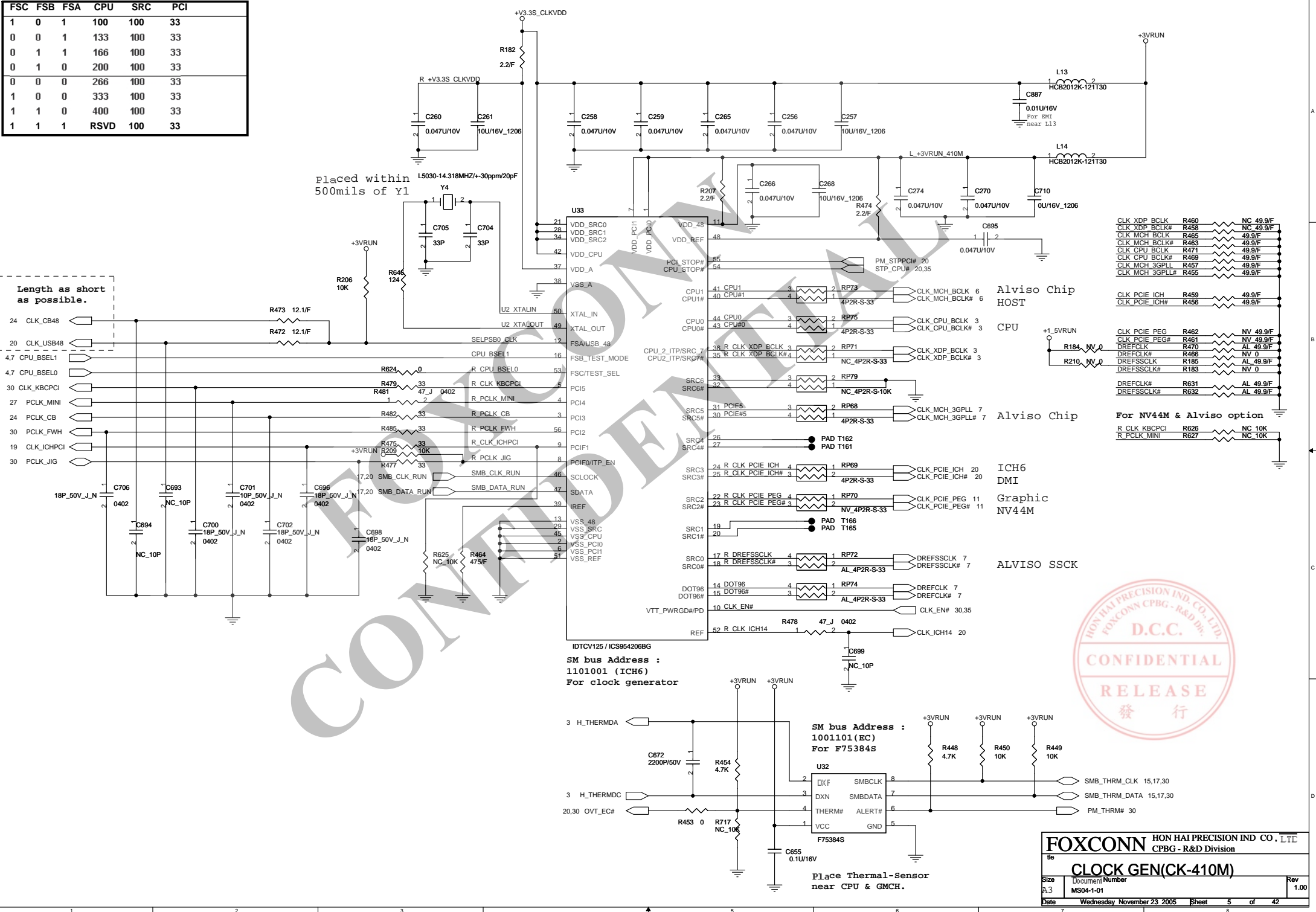
VID



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Placed within  
500mils of Y1

Length as short  
as possible.



CLK_XDP_BCLK	R460	NC	49.9F
CLK_XDP_BCLK#	R458	NC	49.9F
CLK_MCH_BCLK	R465		49.9F
CLK_MCH_BCLK#	R463		49.9F
CLK_CPU_BCLK	R471		49.9F
CLK_CPU_BCLK#	R469		49.9F
CLK_MCH_3GPLL	R457		49.9F
CLK_MCH_3GPLL#	R455		49.9F

CLK_PCIE_ICH	R459		49.9F
CLK_PCIE_ICH#	R456		49.9F

CLK_PCIE_PEG	R462	NV	49.9F
CLK_PCIE_PEG#	R461	NV	49.9F
DREFCLK	R470	AL	49.9F
DREFCLK#	R466	NV	0
DREFSSCLK	R185	AL	49.9F
DREFSSCLK#	R183	NV	0

DREFCLK#	R631		49.9F
DREFSSCLK#	R632		49.9F

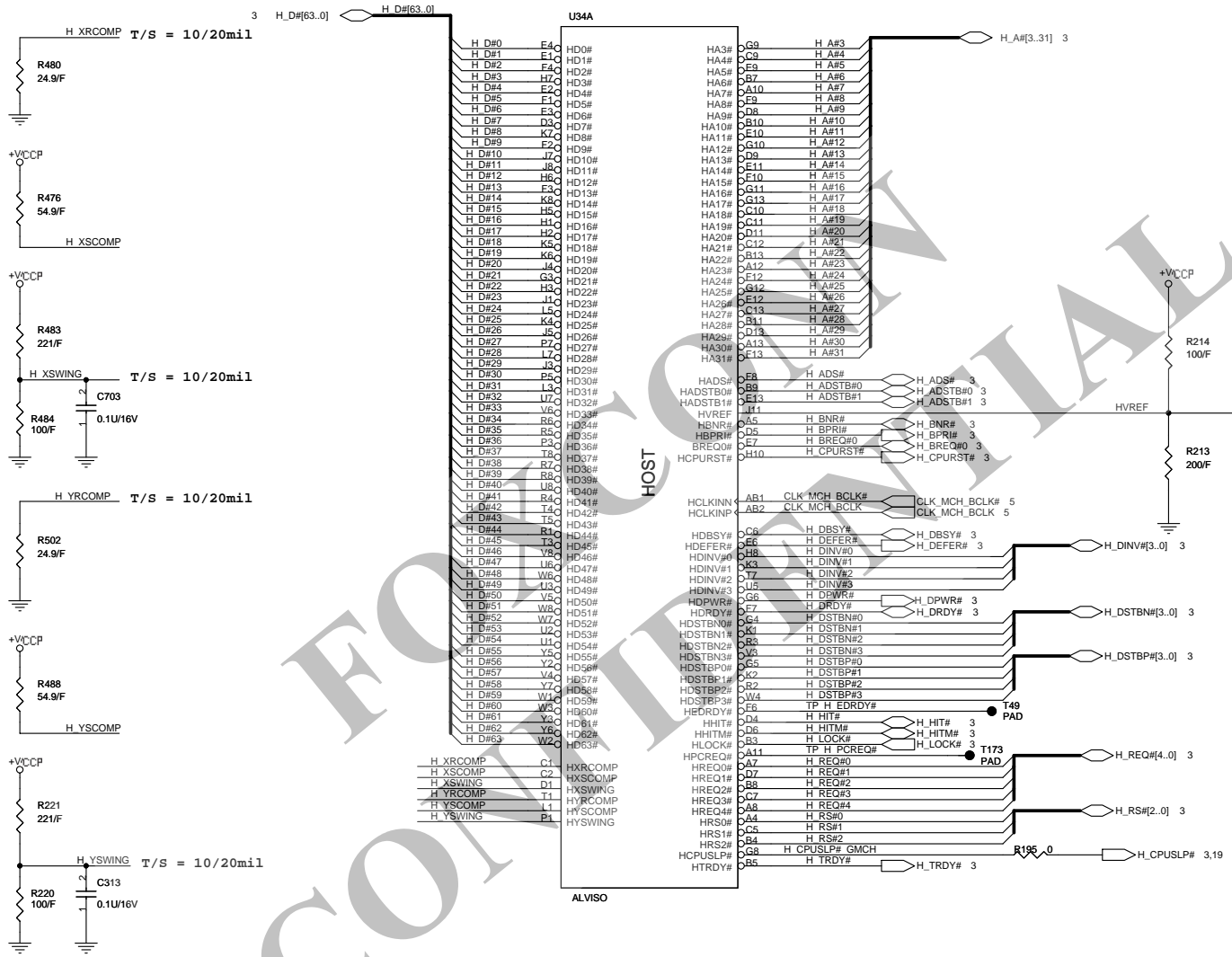
R_CLK_KBCPCI	R626	NC	10K
R_PCLK_MINI	R627	NC	10K

IDTCV125 / ICS954206BG  
SM bus Address :  
11011001 (ICH6)  
For clock generator

SM bus Address :  
1001101 (EC)  
For F75384S

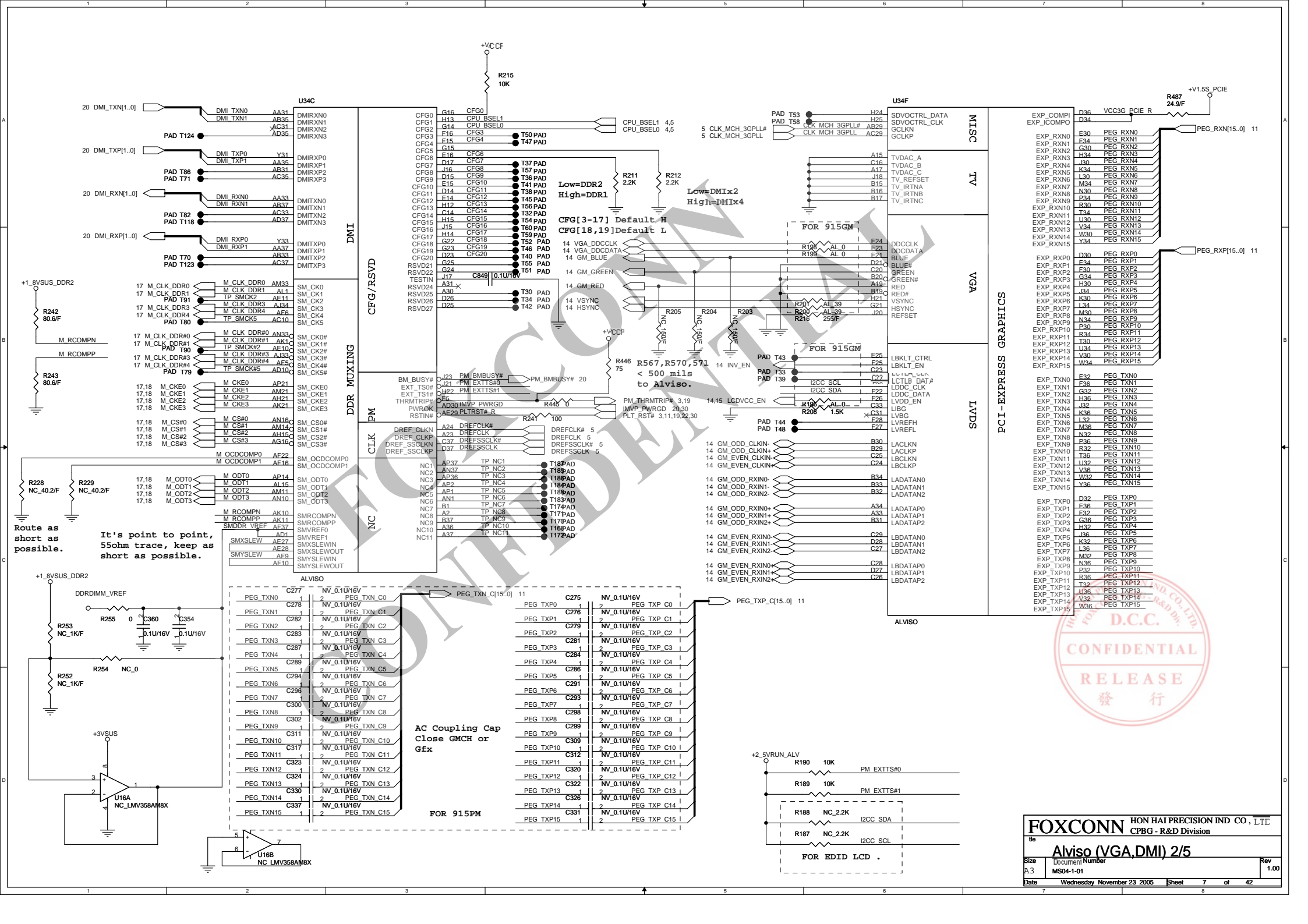


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CLOCK GEN(CK-410M)			
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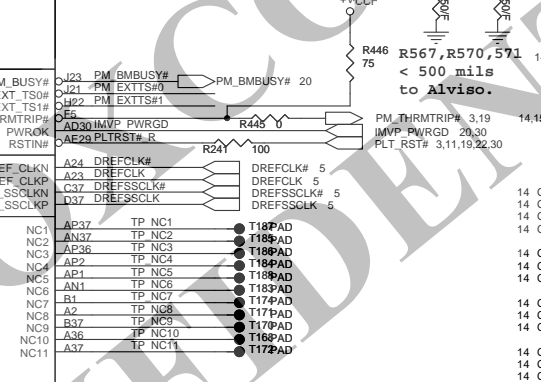
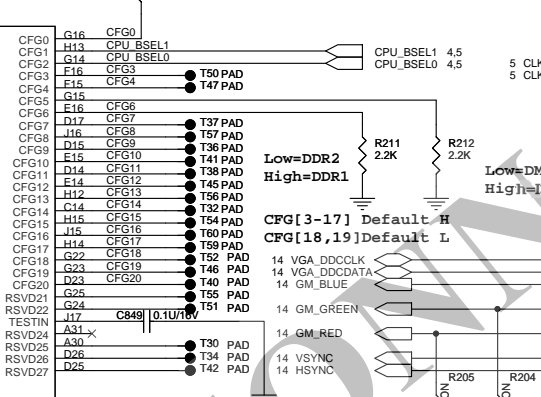
FOXCONN





Route as short as possible.

It's point to point, 55ohm trace, keep as short as possible.



ALVISO

C277	NV_0.1u/16V	PEG_TXN0	PEG_TXN_C0	C275	NV_0.1u/16V	PEG_TXP0	PEG_TXP_C0
C278	NV_0.1u/16V	PEG_TXN1	PEG_TXN_C1	C276	NV_0.1u/16V	PEG_TXP1	PEG_TXP_C1
C282	NV_0.1u/16V	PEG_TXN2	PEG_TXN_C2	C279	NV_0.1u/16V	PEG_TXP2	PEG_TXP_C2
C283	NV_0.1u/16V	PEG_TXN3	PEG_TXN_C3	C281	NV_0.1u/16V	PEG_TXP3	PEG_TXP_C3
C287	NV_0.1u/16V	PEG_TXN4	PEG_TXN_C4	C284	NV_0.1u/16V	PEG_TXP4	PEG_TXP_C4
C289	NV_0.1u/16V	PEG_TXN5	PEG_TXN_C5	C286	NV_0.1u/16V	PEG_TXP5	PEG_TXP_C5
C294	NV_0.1u/16V	PEG_TXN6	PEG_TXN_C6	C291	NV_0.1u/16V	PEG_TXP6	PEG_TXP_C6
C296	NV_0.1u/16V	PEG_TXN7	PEG_TXN_C7	C293	NV_0.1u/16V	PEG_TXP7	PEG_TXP_C7
C300	NV_0.1u/16V	PEG_TXN8	PEG_TXN_C8	C296	NV_0.1u/16V	PEG_TXP8	PEG_TXP_C8
C302	NV_0.1u/16V	PEG_TXN9	PEG_TXN_C9	C299	NV_0.1u/16V	PEG_TXP9	PEG_TXP_C9
C311	NV_0.1u/16V	PEG_TXN10	PEG_TXN_C10	C309	NV_0.1u/16V	PEG_TXP10	PEG_TXP_C10
C317	NV_0.1u/16V	PEG_TXN11	PEG_TXN_C11	C312	NV_0.1u/16V	PEG_TXP11	PEG_TXP_C11
C323	NV_0.1u/16V	PEG_TXN12	PEG_TXN_C12	C320	NV_0.1u/16V	PEG_TXP12	PEG_TXP_C12
C324	NV_0.1u/16V	PEG_TXN13	PEG_TXN_C13	C322	NV_0.1u/16V	PEG_TXP13	PEG_TXP_C13
C330	NV_0.1u/16V	PEG_TXN14	PEG_TXN_C14	C326	NV_0.1u/16V	PEG_TXP14	PEG_TXP_C14
C337	NV_0.1u/16V	PEG_TXN15	PEG_TXN_C15	C331	NV_0.1u/16V	PEG_TXP15	PEG_TXP_C15

FOR 915PM

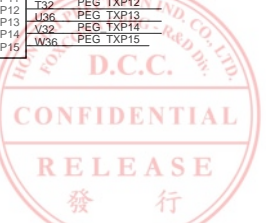
AC Coupling Cap  
Close GMCH or Gfx

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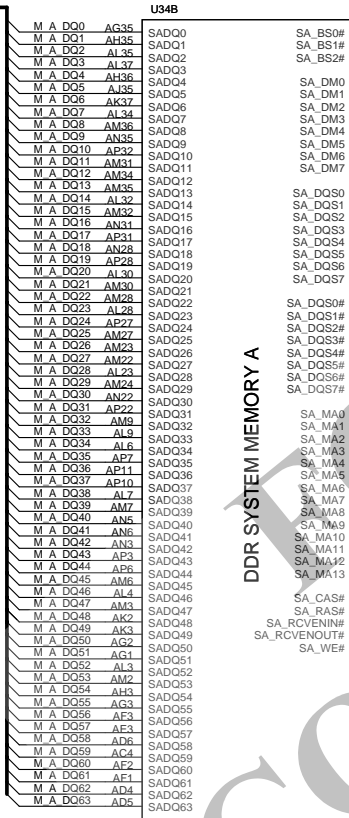
Alviso (VGA, DMI) 2/5

Size A.3 Document Number MS04-1-01 Rev 1.00

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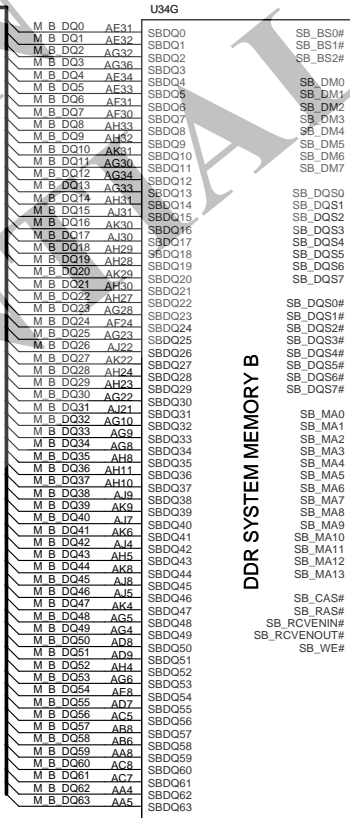


17 M\_A\_DQ[63..0]

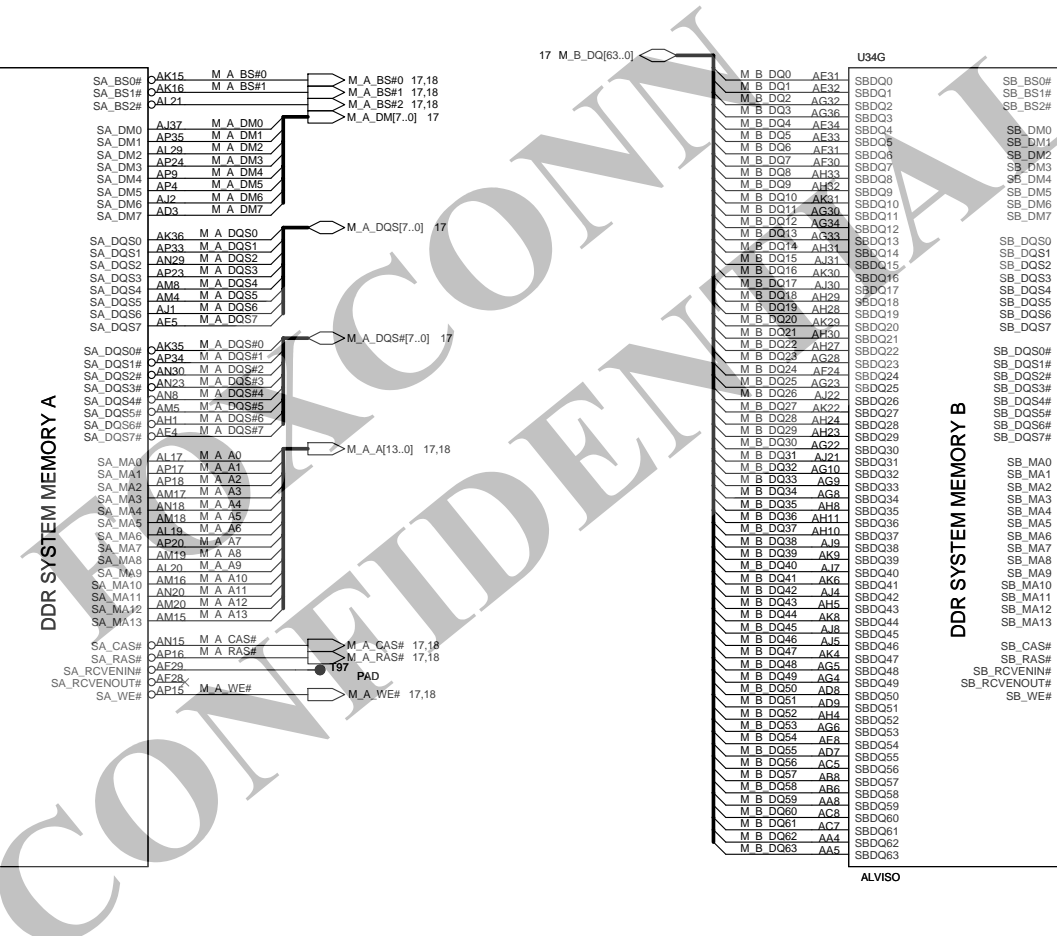


ALVISO

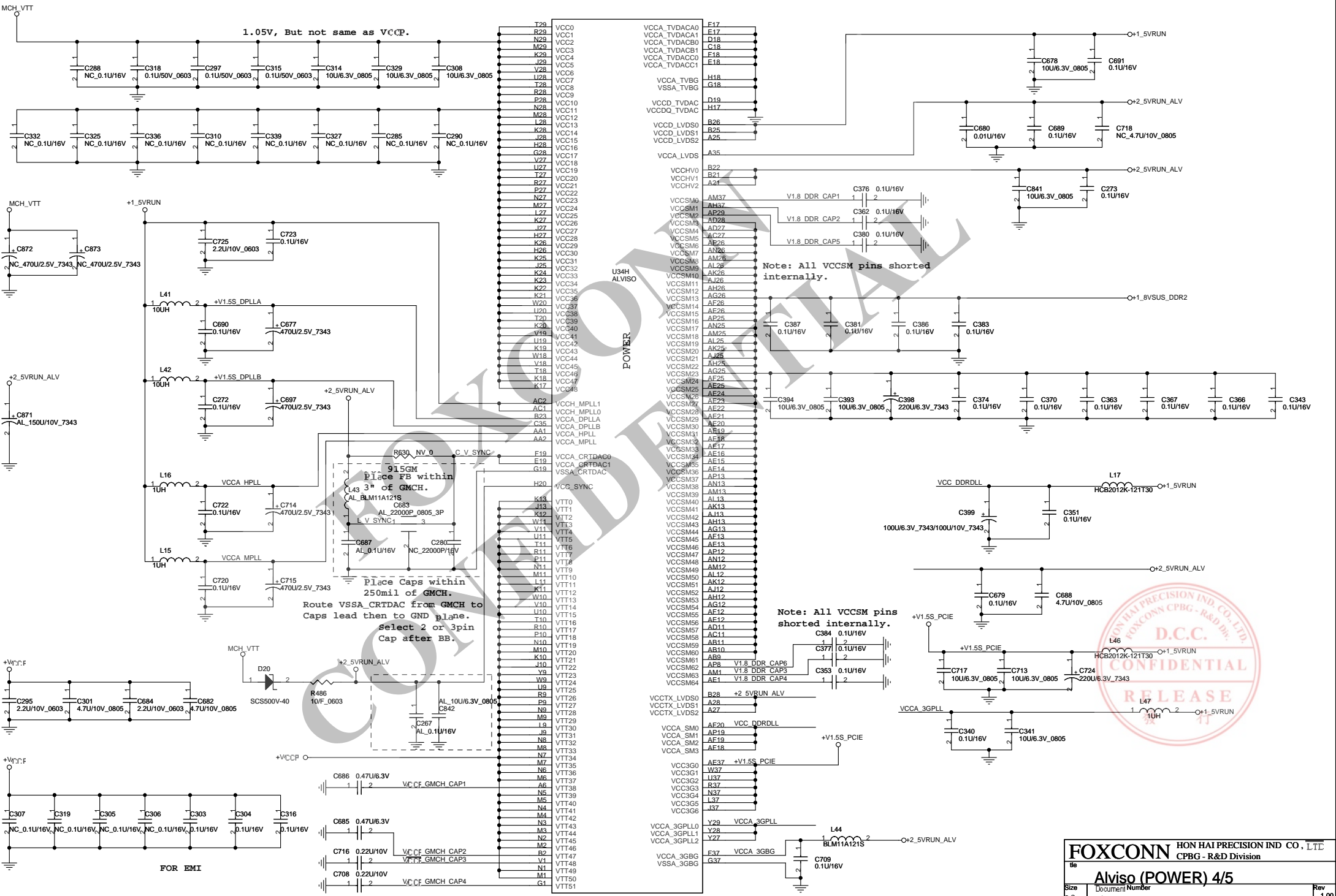
17 M\_B\_DQ[63..0]



ALVISO



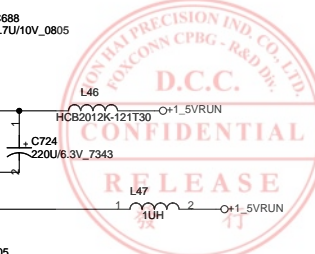


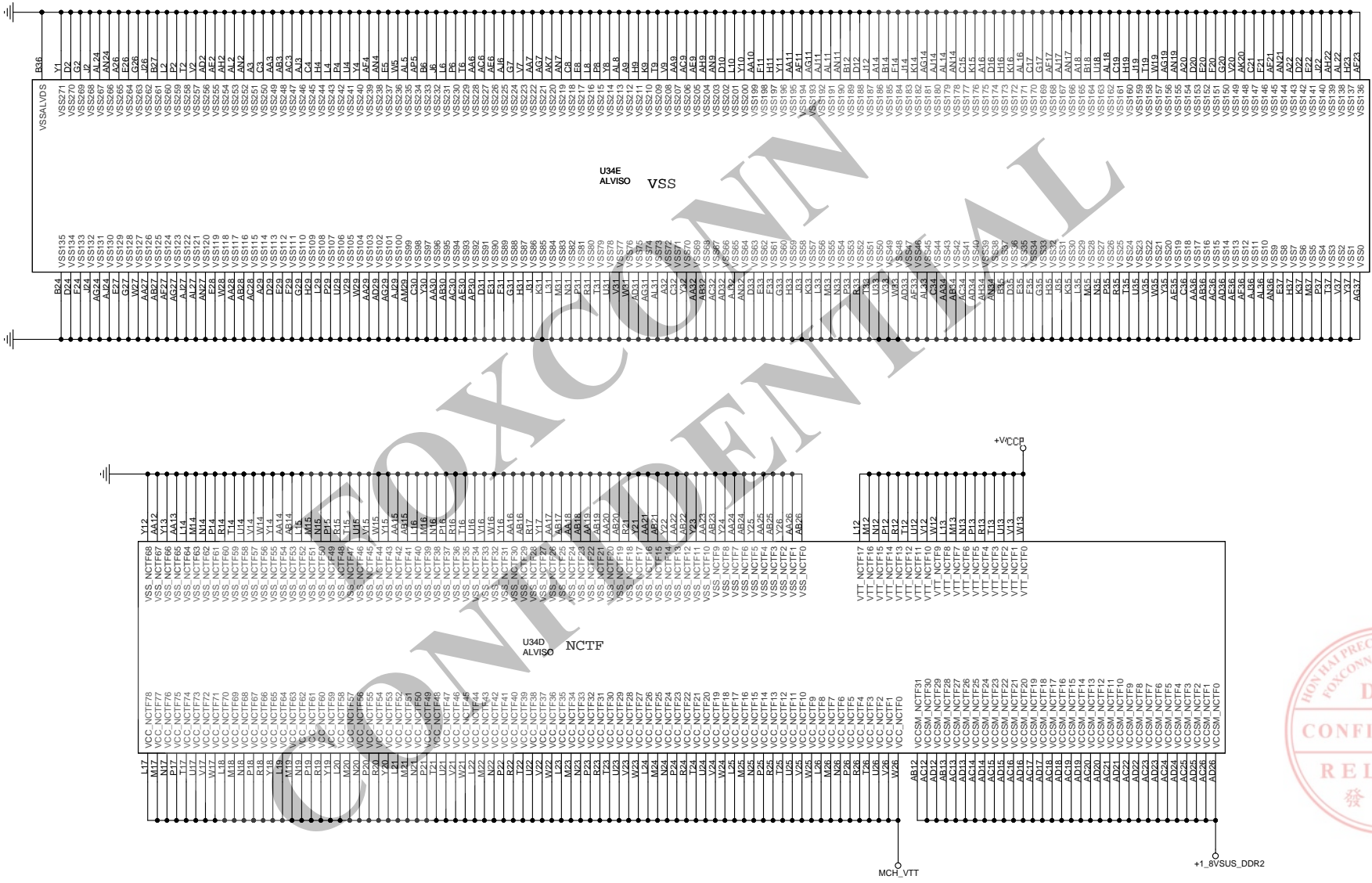


Place FB within 3" of GMCH.  
 Place Caps within 250mil of GMCH.  
 Route VSSA\_CRTDAC from GMCH to Caps lead then to GND plane.  
 Select 2 or 3pin Cap after BB.

Note: All VCCSM pins shorted internally.

Note: All VCCSM pins shorted internally.



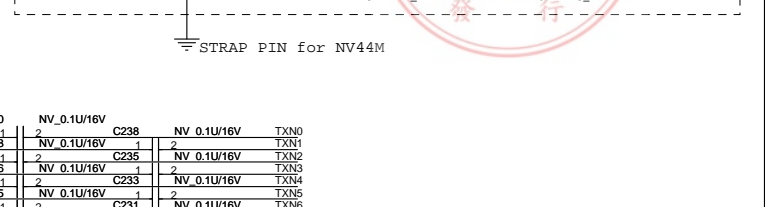
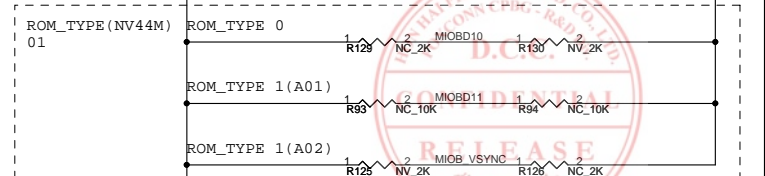
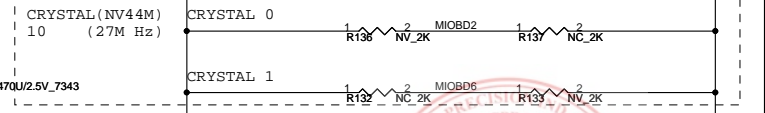
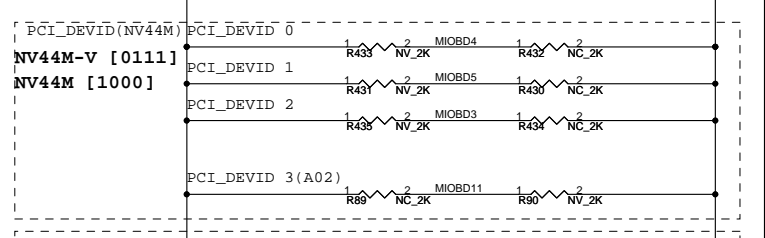
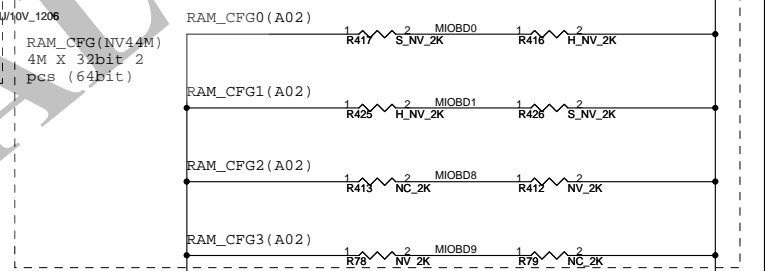
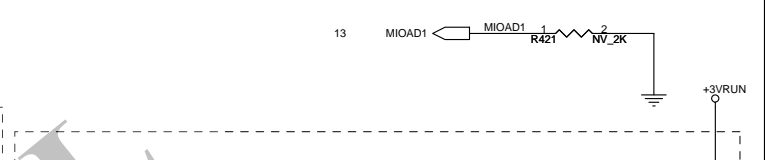
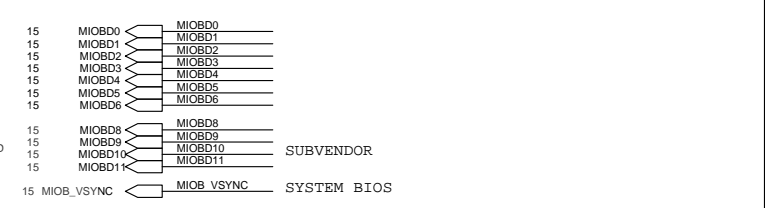
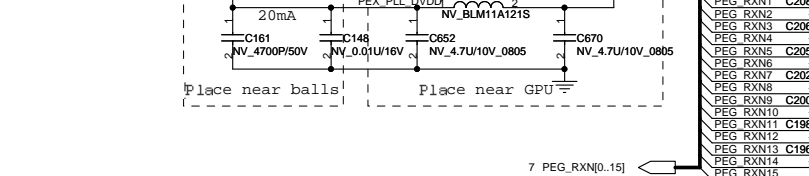
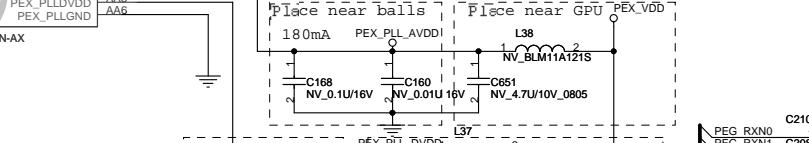
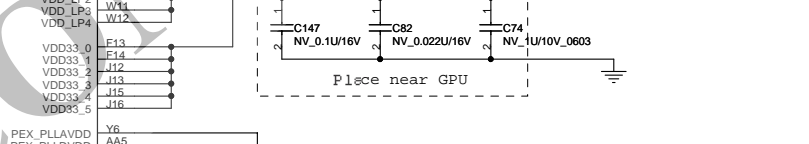
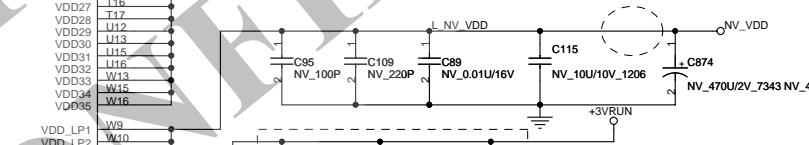
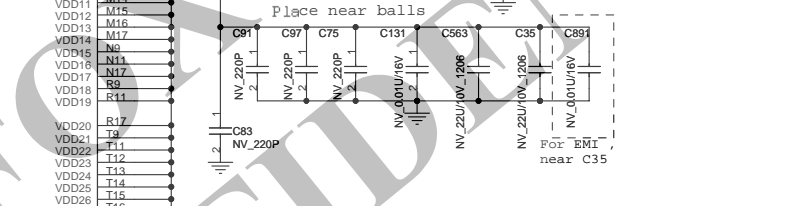
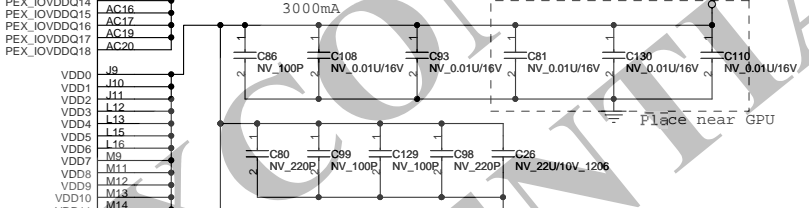
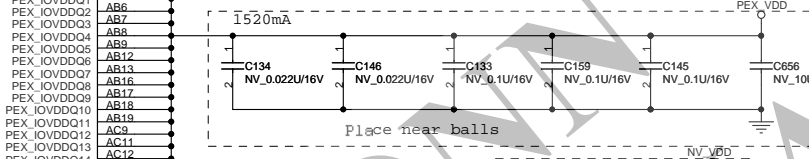
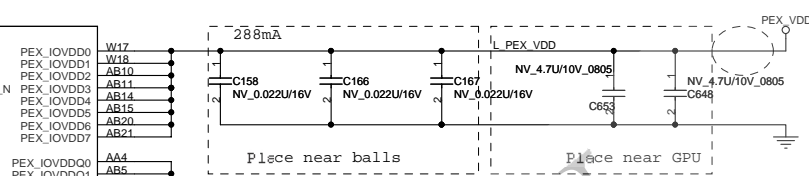
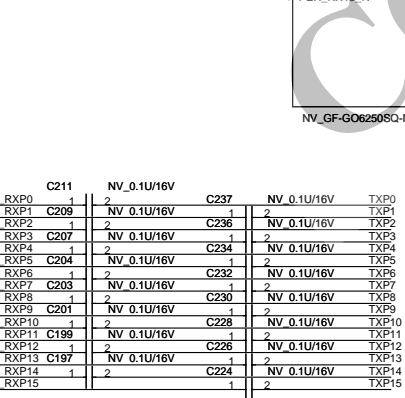
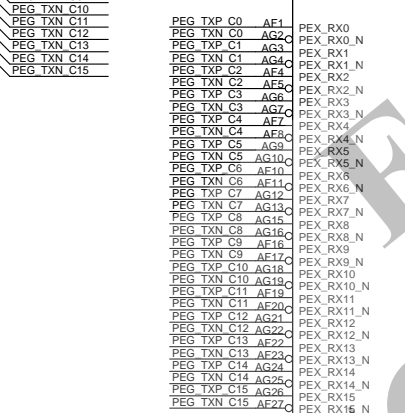
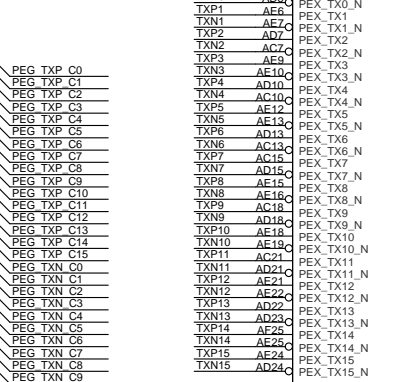
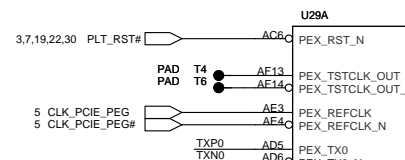


U34E  
ALVISO VSS

U34D  
ALVISO NCTF

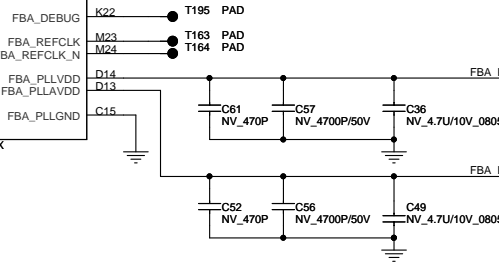
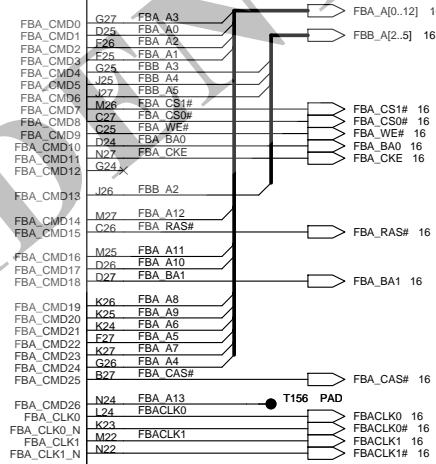
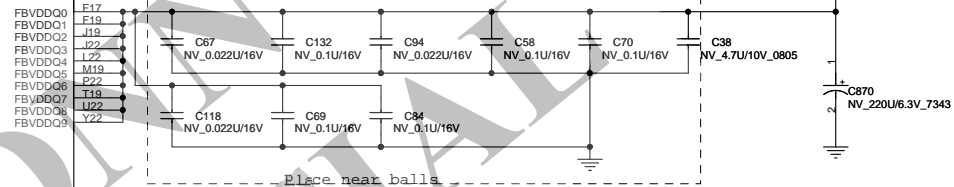
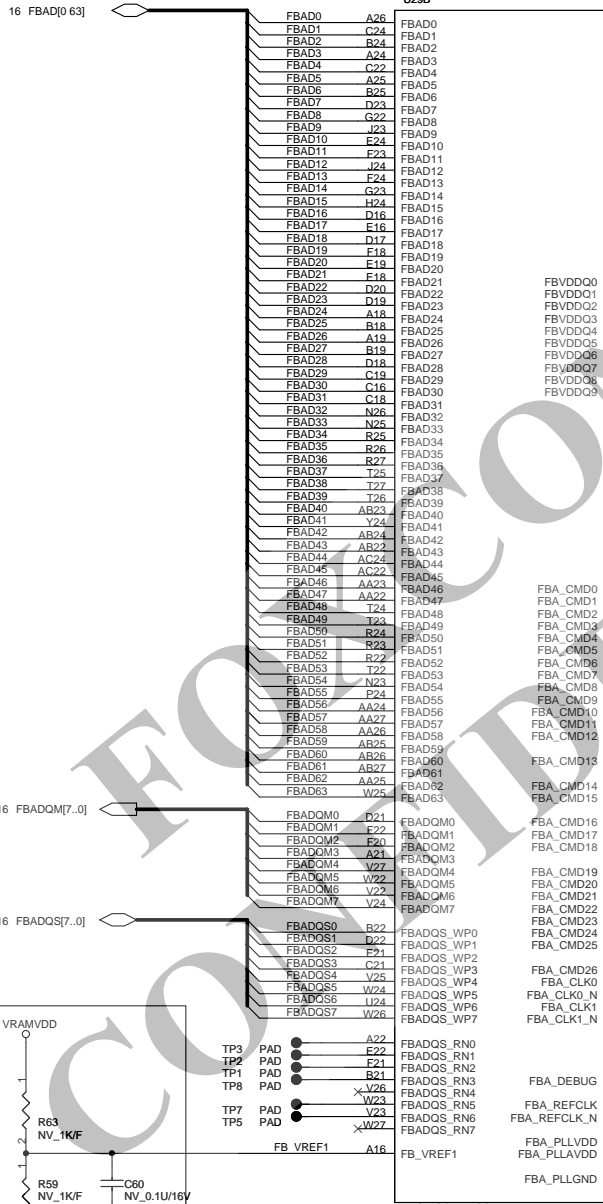
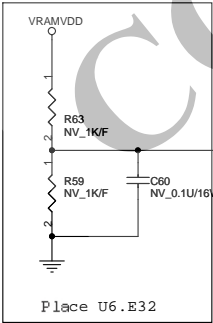
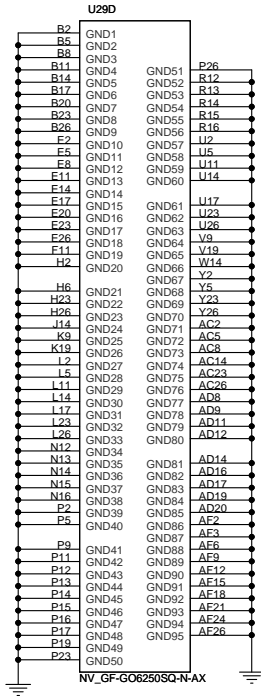


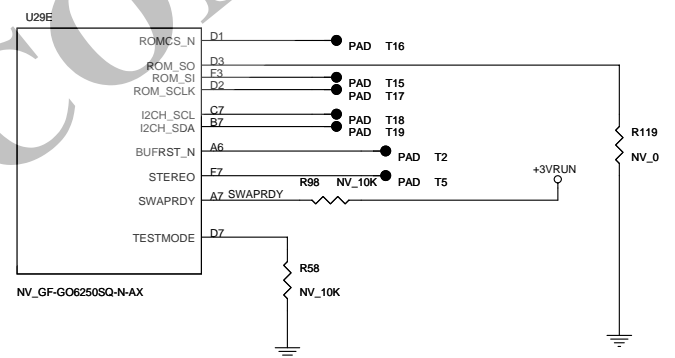
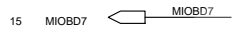
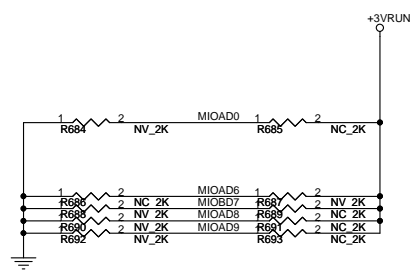
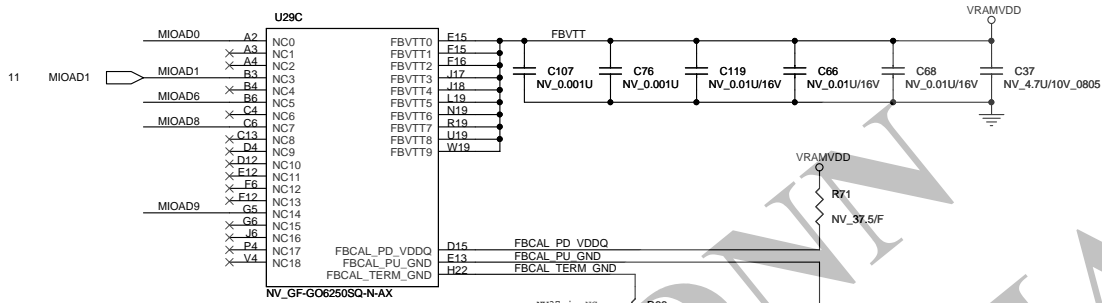
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CPBG - R&D Division			
Alviso (VSS,NCTF) 5/5			
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PEG_RXN0	C210	NV_0.1U/16V	C238	NV_0.1U/16V	TXN0
PEG_RXN1	C208	NV_0.1U/16V	C235	NV_0.1U/16V	TXN1
PEG_RXN2	C206	NV_0.1U/16V	C233	NV_0.1U/16V	TXN2
PEG_RXN3	C204	NV_0.1U/16V	C231	NV_0.1U/16V	TXN3
PEG_RXN4	C202	NV_0.1U/16V	C229	NV_0.1U/16V	TXN4
PEG_RXN5	C200	NV_0.1U/16V	C227	NV_0.1U/16V	TXN5
PEG_RXN6	C198	NV_0.1U/16V	C225	NV_0.1U/16V	TXN6
PEG_RXN7	C196	NV_0.1U/16V	C223	NV_0.1U/16V	TXN7
PEG_RXN8	C194	NV_0.1U/16V	C221	NV_0.1U/16V	TXN8
PEG_RXN9	C192	NV_0.1U/16V	C219	NV_0.1U/16V	TXN9
PEG_RXN10	C190	NV_0.1U/16V	C217	NV_0.1U/16V	TXN10
PEG_RXN11	C188	NV_0.1U/16V	C215	NV_0.1U/16V	TXN11
PEG_RXN12	C186	NV_0.1U/16V	C213	NV_0.1U/16V	TXN12
PEG_RXN13	C184	NV_0.1U/16V	C211	NV_0.1U/16V	TXN13
PEG_RXN14	C182	NV_0.1U/16V	C209	NV_0.1U/16V	TXN14
PEG_RXN15	C180	NV_0.1U/16V	C207	NV_0.1U/16V	TXN15

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**VGA(nVIDIA NV44M) 1/5**  
 Size A.3 Document Number MS04-1-01 Rev 1.00  
 Date Wednesday November 23 2005 Sheet 11 of 42





FOXC CONFI DENTIAL

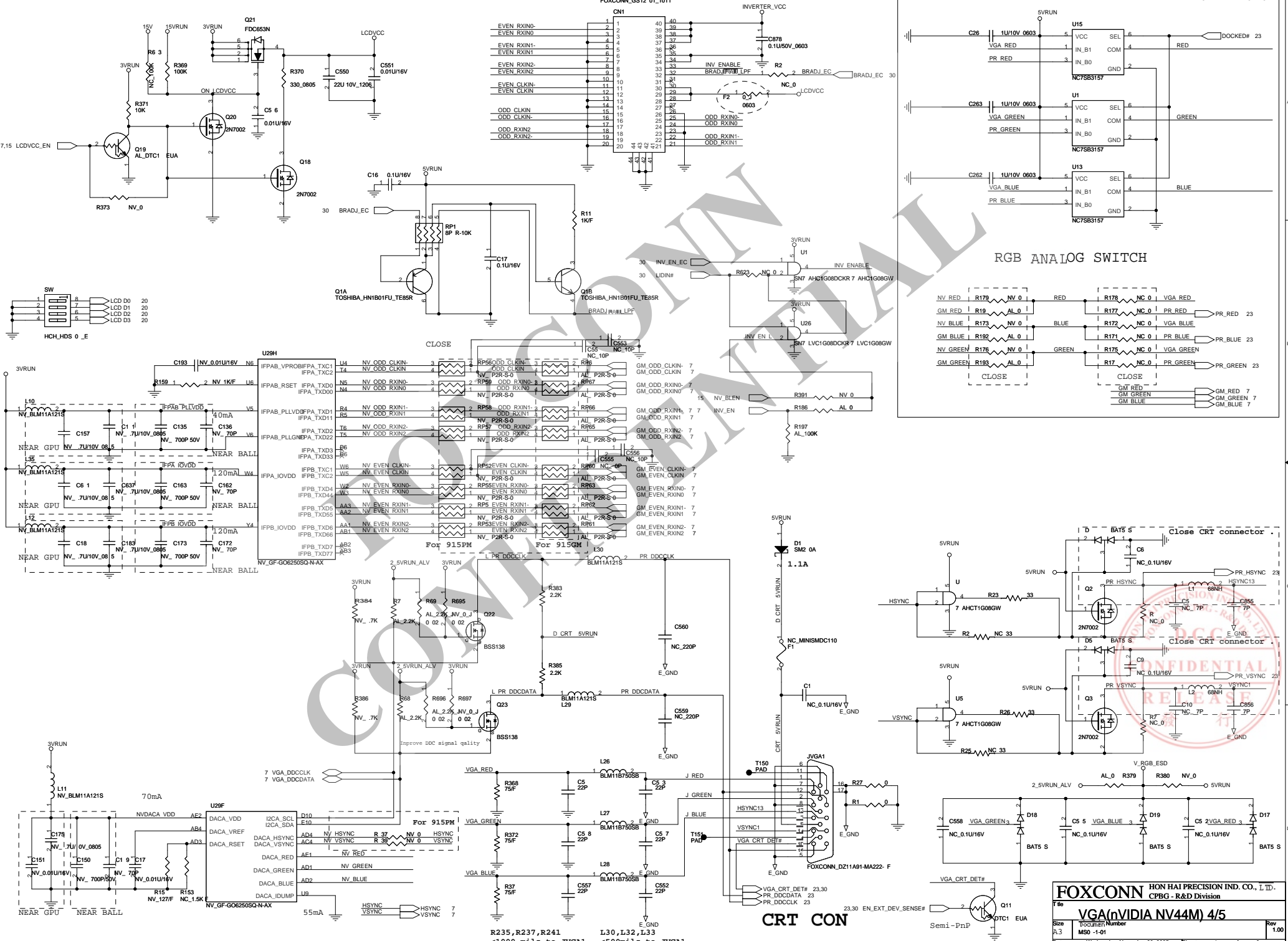


FOXCONN HON HAI PRECISION IND CO, LTD			
CPBG - R&D Division			
File <b>VGA(nVIDIA NV44M) 3/5</b>			
Size A.3	Document Number MS04-1-01	Rev 1.00	
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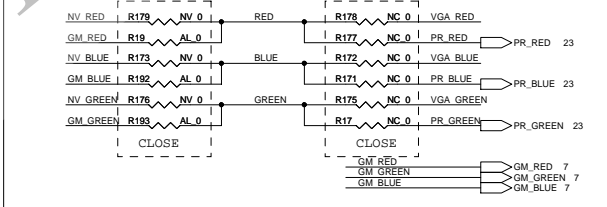
# LVDS CONNECTOR

FOXCONN\_GS12 01\_1011

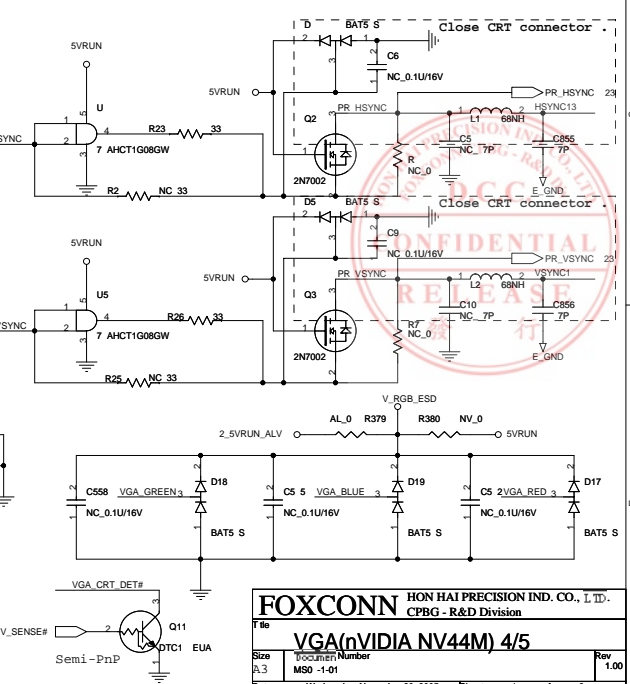
H : NOTEBOOK  
L : PORT REPLICATOR



## RGB ANALOG SWITCH

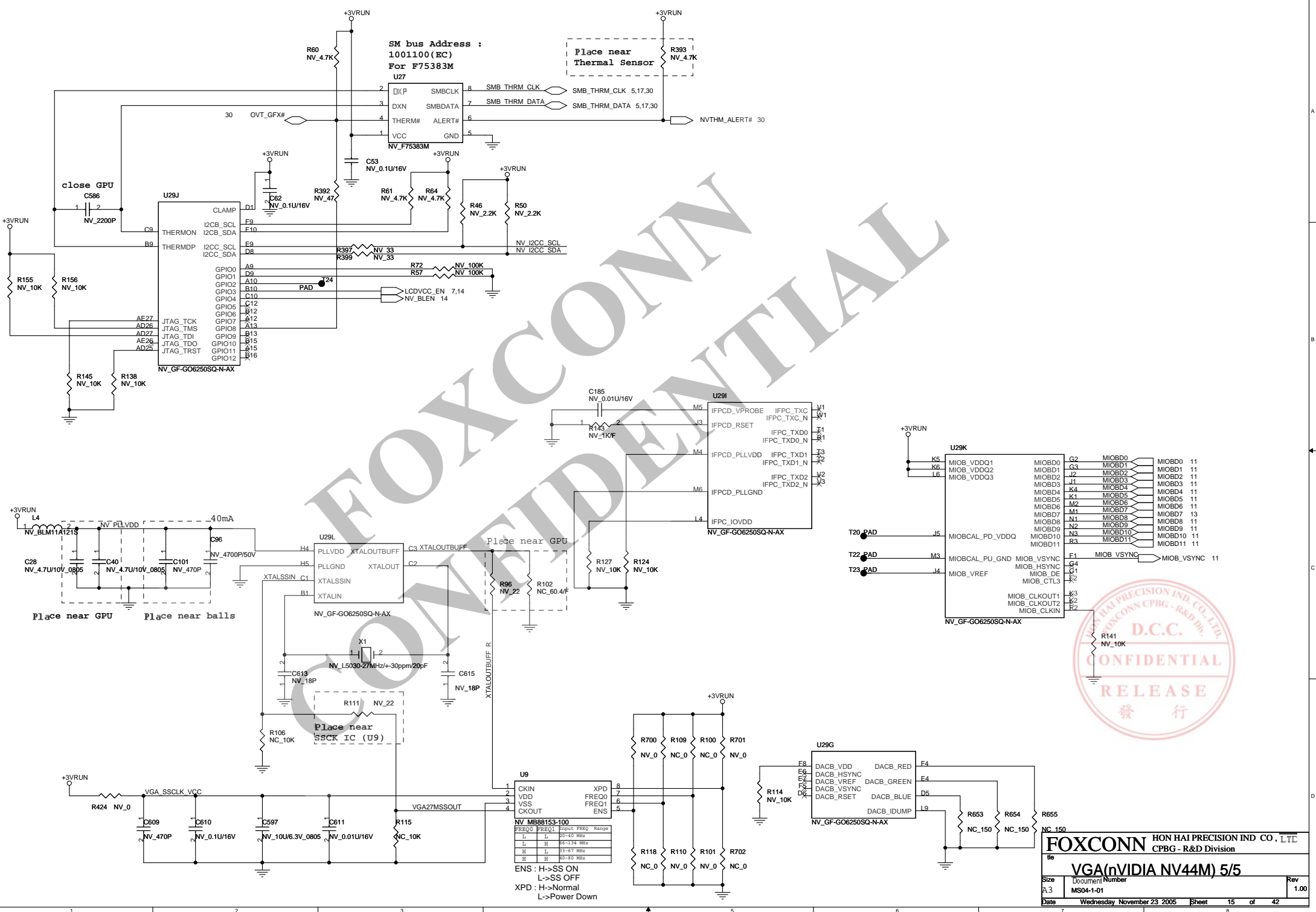


## CRT CON



<b>FOXCONN</b> HON HAI PRECISION IND. CO., L.T.D. CPBG - R&D Division	
File: <b>VGA(nVIDIA NV44M) 4/5</b>	
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R235, R237, R241 L30, L32, L33  
<1000 mils to JVGAL. <500mils to JVGAL.



SM bus Address :  
1001100(EC)  
For F75383M  
U27

Place near  
Thermal Sensor

Place near GPU

Place near GPU Place near balls

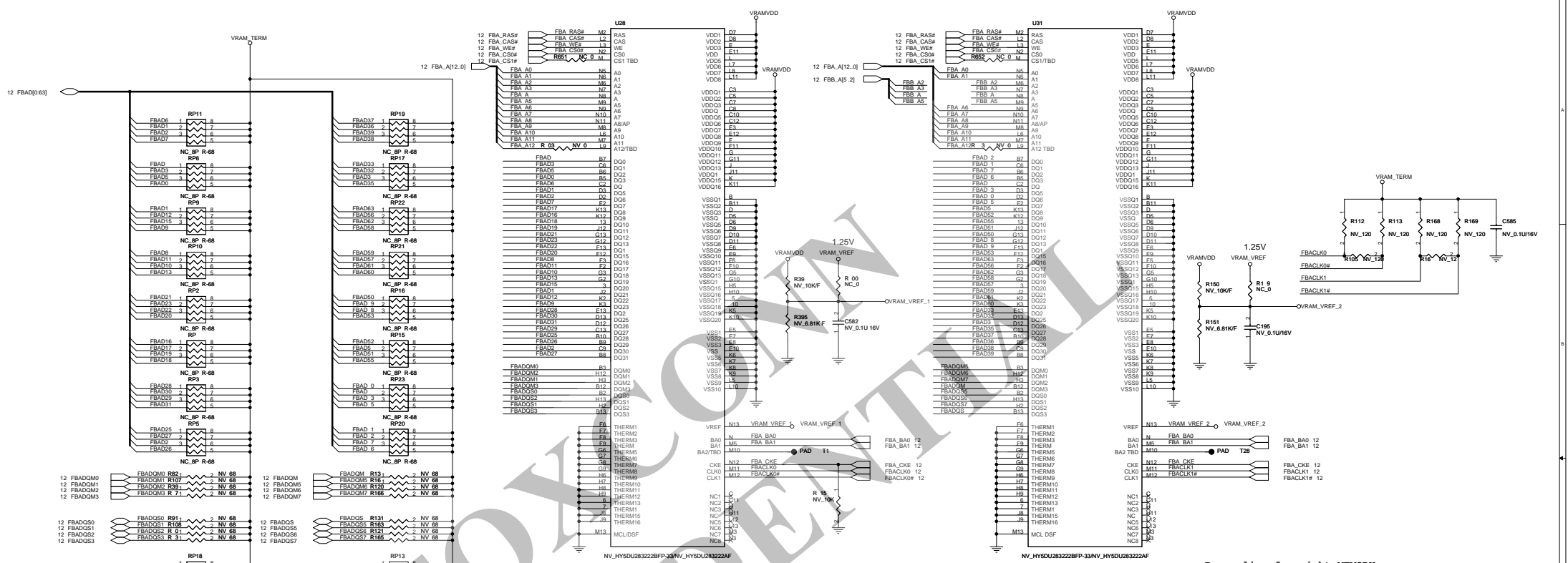
Place near  
SSCK IC (U9)

U9

FREQ0	FREQ1	FREQ2	FREQ3	FREQ4	FREQ5	FREQ6	FREQ7	FREQ8	FREQ9
L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H	H	H

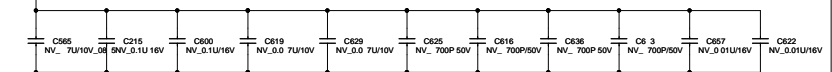
ENS : H->SS ON  
L->SS OFF  
XPD : H->Normal  
L->Power Down



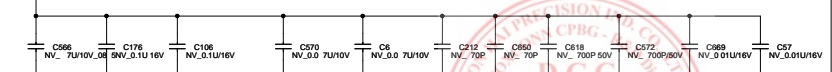


**Decoupling for right MEMORY**

Place around the MEM

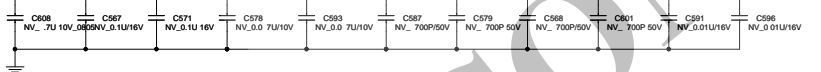


Place under the MEM

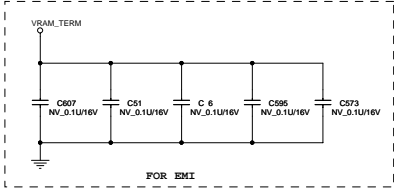
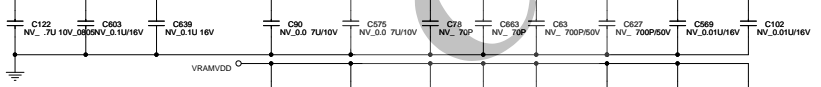


**Decoupling for left MEMORY**

Place around the MEM



Place under the MEM



FOR EM1

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File: **NV44M(DDR F A B 1)**

Rev: 1.3

Drawn: MSO -1-01

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