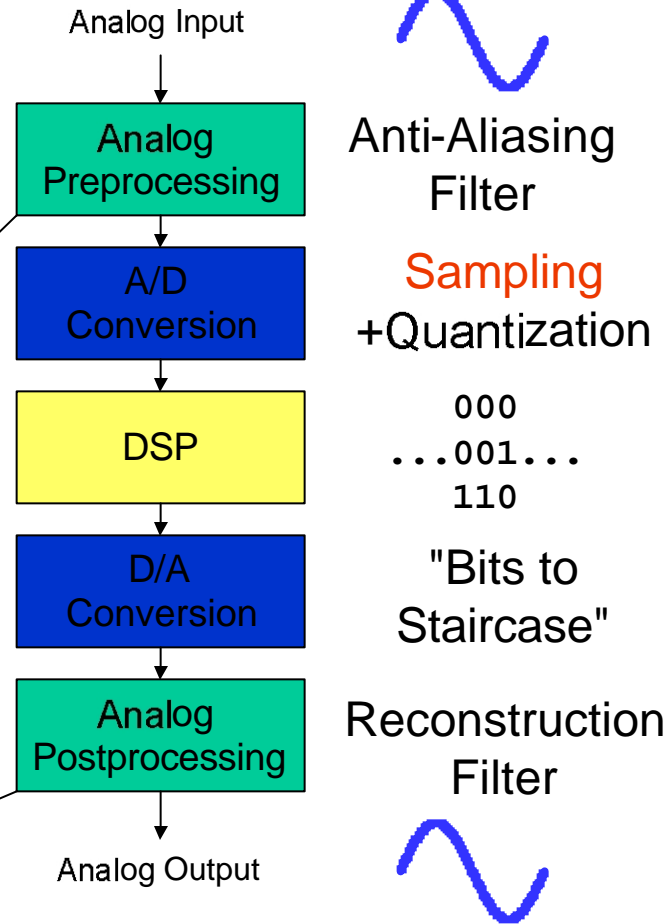


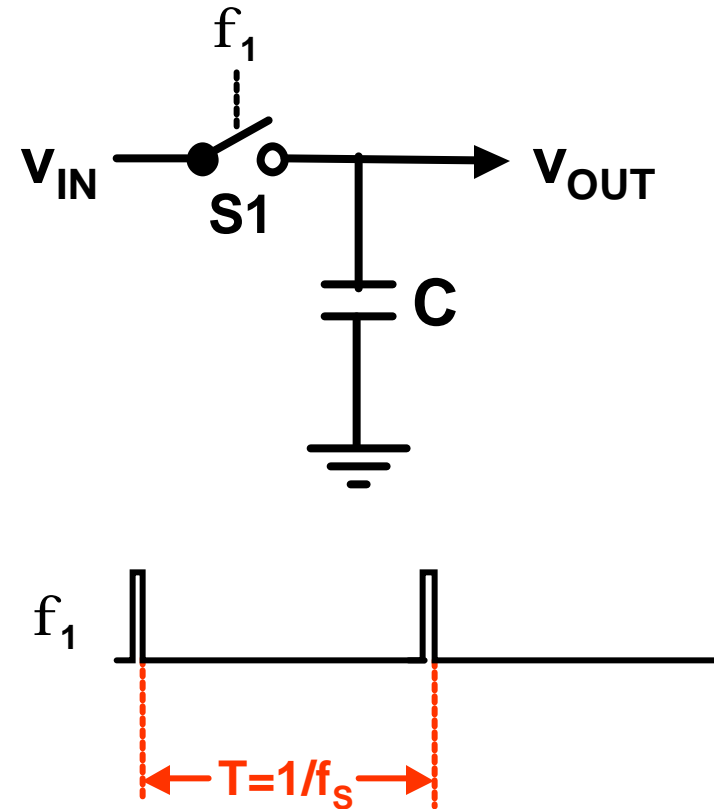
Re-Cap

- How can we build circuits that "sample"

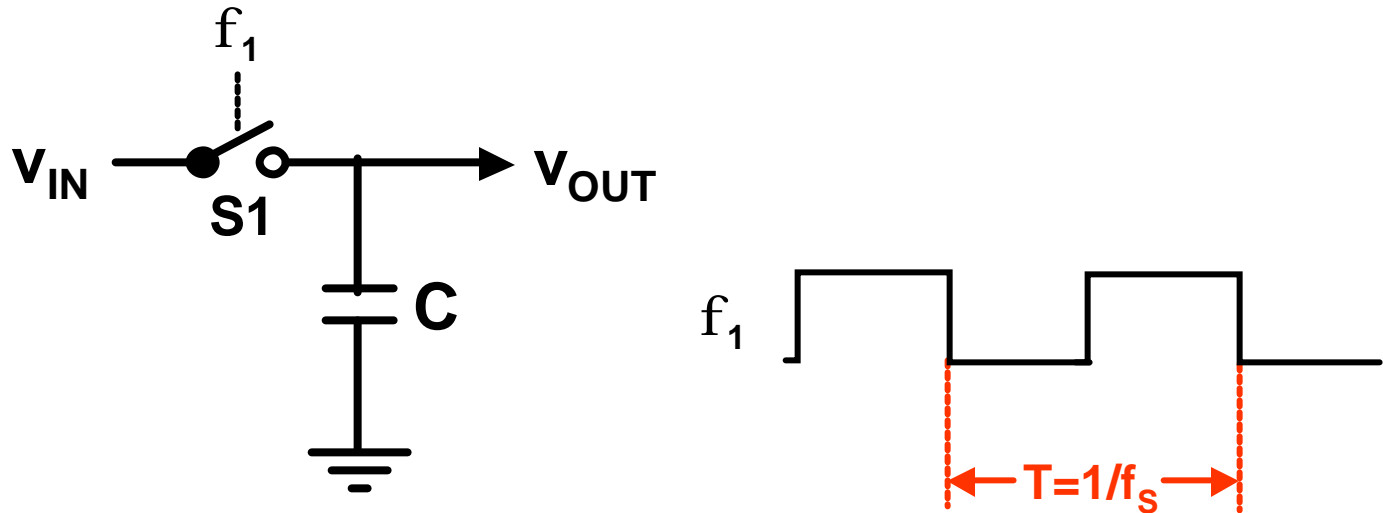


Ideal Sampling

- In an ideal world, zero resistance sampling switches would close for the briefest instant to sample a continuous voltage v_{IN} onto the capacitor C
- Not realizable!



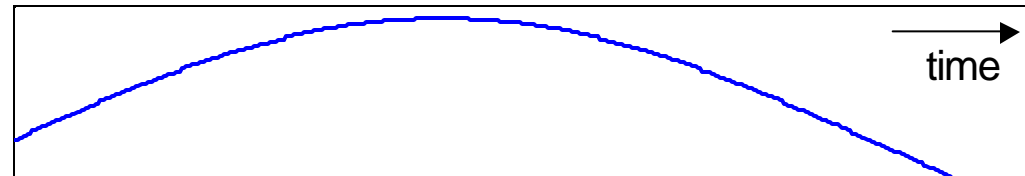
Ideal T/H Sampling



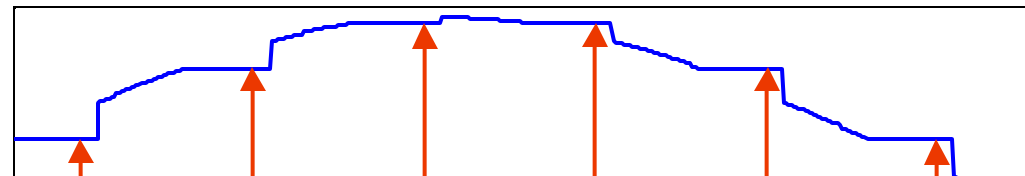
- V_{out} tracks input when switch is closed
- Grab *exact* value of V_{in} when switch opens
- "Track and Hold" (T/H)

Ideal T/H Sampling

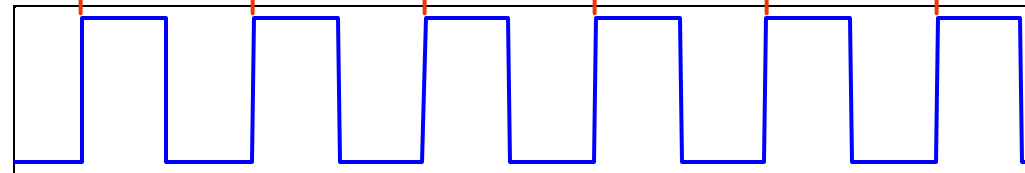
Continuous
Time



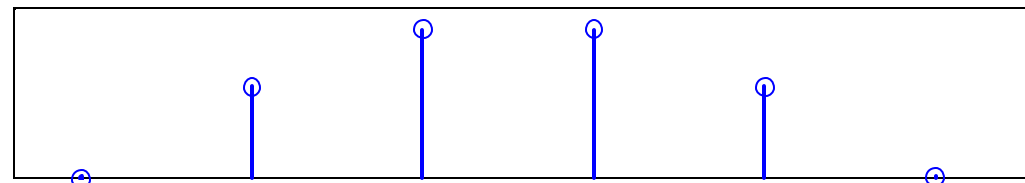
T/H signal
(SD Signal)



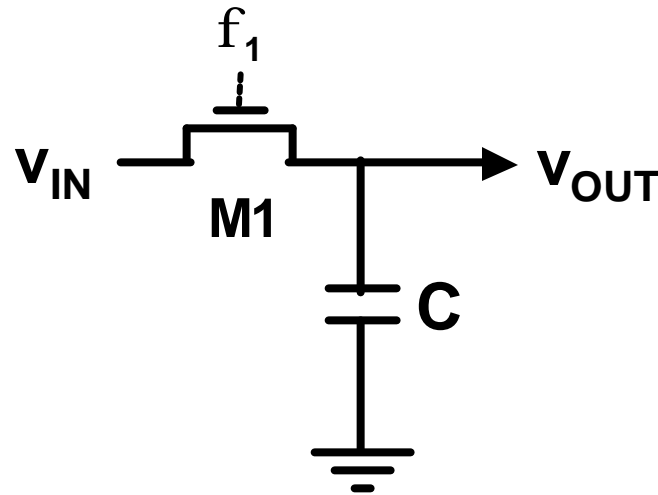
Clock



DT Signal



Practical Sampling



- kT/C noise
- Finite $R_{sw} \rightarrow$ limited bandwidth
- $R_{sw} = f(V_{in}) \rightarrow$ distortion
- Switch charge injection (EE240)
- Clock jitter

kT/C Noise

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

$$C \geq 12k_B T \left(\frac{2^B - 1}{V_{FS}} \right)^2$$

In high resolution ADCs kT/C noise usually dominates overall error (power dissipation argument).

B	C_{\min} ($V_{FS} = 1V$)
8	0.003 pF
12	0.8 pF
14	13 pF
16	206 pF
20	52,800 pF

以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：<https://d.book118.com/905020243204011224>