Copyright © HiSilicon Technologies Co., Ltd. 2013. All rights reserved.

No part of this document may be reproduced or transmitted in any form or by any means without prior written consent of HiSilicon Technologies Co., Ltd.

Trademarks and Permissions

 , HISILICON, and other HiSilicon icons are trademarks of HiSilicon Technologies Co., Ltd.

All other trademarks and trade names mentioned in this document are the property of their respective holders.

Notice

The purchased products, services and features are stipulated by the contract made between HiSilicon and the customer. All or part of the products, services and features described in this document may not be within the purchase scope or the usage scope. Unless otherwise specified in the contract, all statements, information, and recommendations in this document are provided "AS IS" without warranties, guarantees or representations of any kind, either express or implied.

The information in this document is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents, but all statements, information, and recommendations in this document do not constitute a warranty of any kind, express or implied.

HiSilicon Technologies Co., Ltd.

Address: Huawei Industrial Base
Bantian, Longgang
Shenzhen 518129
People's Republic of China

Website: http://www.hisilicon.com

Email: support@hisilicon.com

About This Document

Purpose

This document describes the recommendations for Hi3520D/Hi3515A/Hi3515C schematic diagram design, PCB design, and board thermal design.

This document provides hardware design methods for the Hi3520D/Hi3515A/Hi3515C.

Related Version

The following table lists the product version related to this document:

Product Name	Related Version
Hi3520D	V100
Hi3515A	V100
Hi3515C	V100

Intended Audience

This document is intended for:

- Technical support personnel
- Board hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 03 (2013-07-31)

This issue is the third official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

In section 1.2.4, the descriptions of Ethernet port indicators are added.

In section 1.3.1, the pins HDMI_HOTPLUG, HDMI_CEC, HDMI_SCL, and HDMI_SDA are added to Table 1-5.

Issue 02 (2013-06-21)

This issue is the second official release, which incorporates the following changes:

The descriptions related to the Hi3515C are added.

Issue 01 (2013-05-21)

This issue is the first official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

Section 1.2.2 "RTC" is added.

In section 1.2.12, a note is added.

Chapter 2 PCB Design Recommendations

In section 2.1.1, the descriptions of the impedance design are updated.

Chapter 3 Recommendations for Board Thermal Design

The heat dissipation solution for the Hi3520D is added.

Issue 00B03 (2013-04-03)

This issue is the first draft release.

Copyright © HiSilicon Technologies Co., Ltd

Contents

HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

Figures

HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

Tables

HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

1 Design Recommendations for Schematic Diagrams

NOTE

Unless otherwise specified, this document applies to the Hi3520D, Hi3515A and Hi3515C and uses the Hi3520D as an example.

1.1 Requirements on Circuits for the Small System

1.1.1 Clocking Circuit

The system clock can be generated by combining the internal feedback circuit of the Hi3520D with an external 24 MHz crystal oscillator circuit.

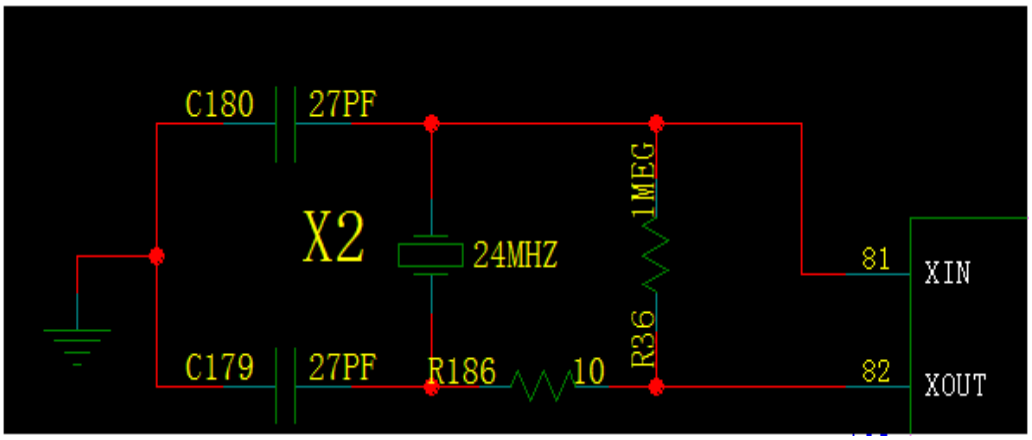
Figure 1-1 shows the recommended connection mode of the crystal oscillator and component specifications for the system clock.

CAUTION

The selected capacitors must match the load capacitor of the crystal oscillator, and the capacitor material should be NPO.

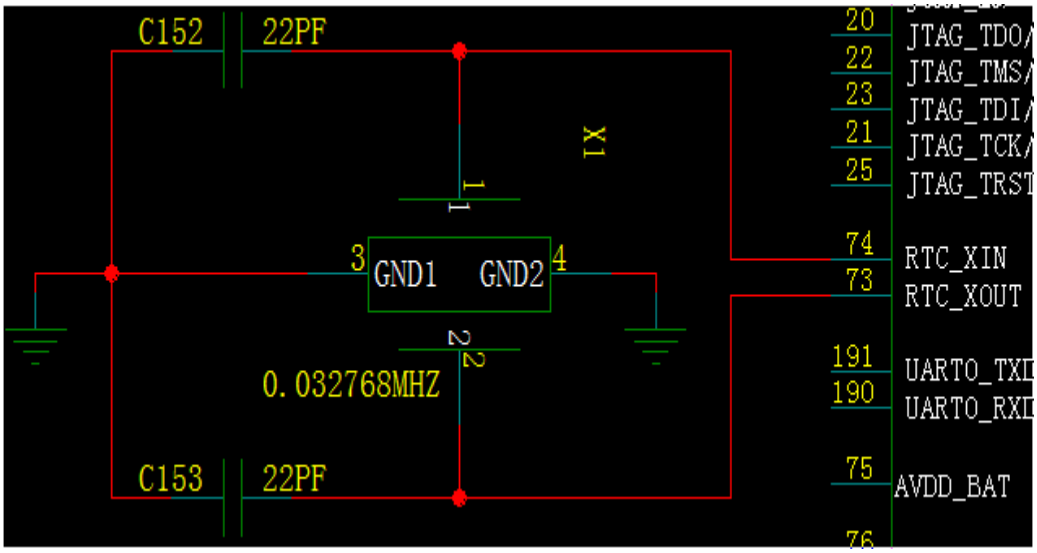
HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

Figure 1-1 Recommended connection mode of the crystal oscillator and component specifications for the system clock



The Hi3520D integrates an RTC, to which a crystal oscillator on the board must provide a clock circuit. Figure 1-2 shows the recommended connection mode of the crystal oscillator and component specifications for the RTC.

Figure 1-2 Recommended connection mode of the crystal oscillator and component specifications for the RTC



1.1.2 Reset and Watchdog Circuits

The Hi3520D RSTN pin is a reset signal input pin. The valid reset signal must have low-level pulses with a typical width of 100–300 ms.

During board design, you are advised to use a dedicated reset chip to generate reset signals to ensure system stability. If a Hi3520D reset exception occurs, the Hi3520D can generate low-level pulses through the WDG_RSTN pin, which connects to an input pin on the reset chip to reset the Hi3520D system.

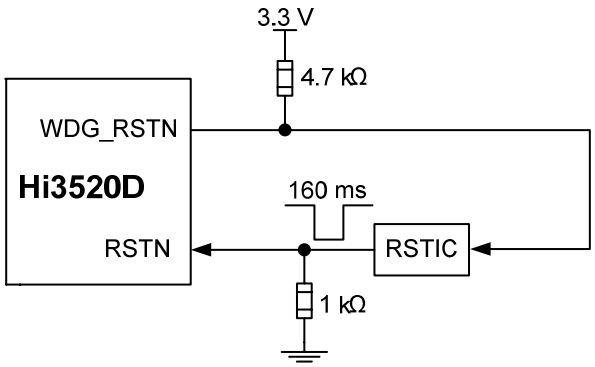
HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

CAUTION

The WDG_RSTN pin is an OD output and must connect to an external pull-up resistor. This pin cannot directly connect to the RSTN pin.

Figure 1-3 shows the typical reset and watchdog circuit.

Figure 1-3 Typical reset and watchdog circuit



1.1.3 JTAG Debug Interface

The Hi3520D provides a JTAG debug interface that complies with the IEEE1149.1 standard. PCs can connect to a Realview-ICE simulator over this interface. Table 1-1 describes the signals over the JTAG debug interface.

Table 1-1 Signals over the JTAG debug interface

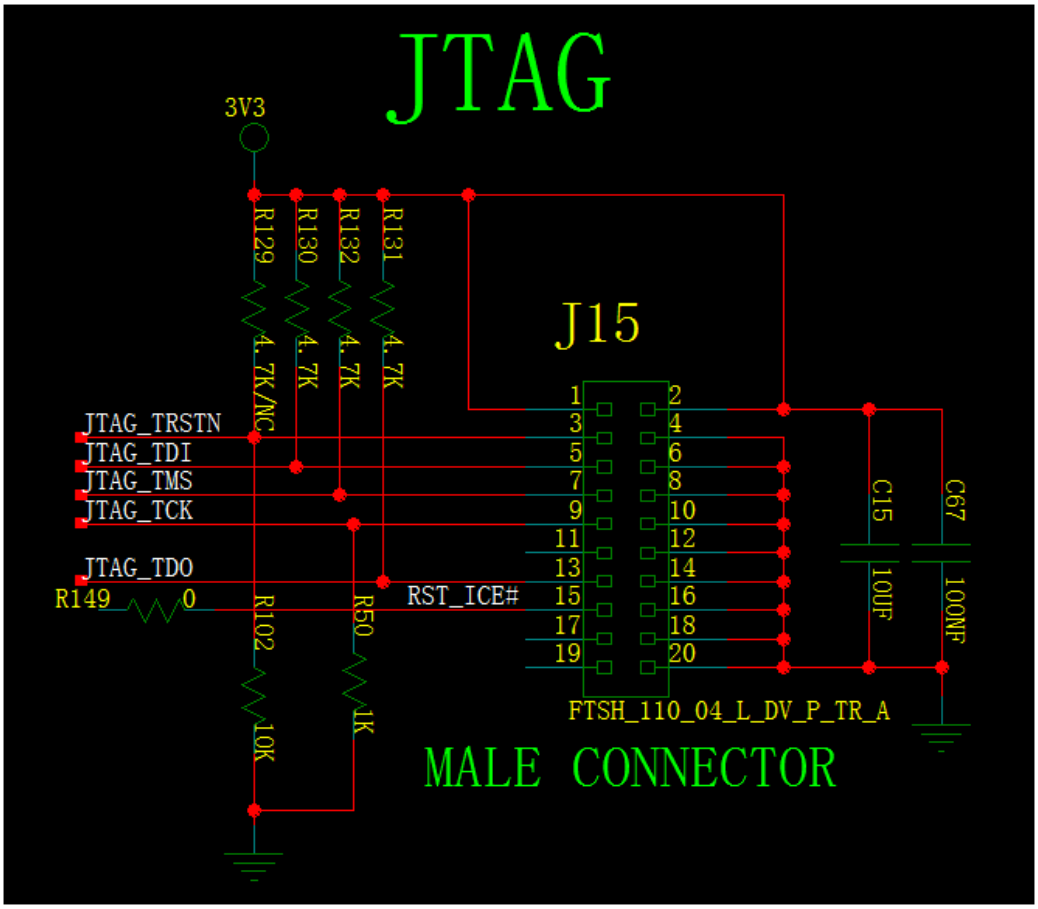
Signal	Description
TCK	JTAG clock input, internal pull-down. A pull-down resistor must connect to this signal on the board.
TDI	JTAG data input, internal pull-up. A pull-up resistor must connect to this signal on the board.
TMS	JTAG mode select input, internal pull-up. A pull-up resistor must connect to this signal on the board.
TRSTN	JTAG reset input, internal pull-down. When the Hi3520D works properly, a pull-down resistor must connect to this signal on the board.
TDO	JTAG data output. A pull-up resistor must connect to this signal on the board.

NOTE

For details about the impedance of the external pull-up and pull-down resistors, see Figure 1-4.

HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

Figure 1-4 JTAG connection mode and standard connector pins



The JTAG pins on the Hi3520D can be multiplexed with GPIO pins by configuring the JTAG_EN pin.

The Hi3520D works in normal or test mode, which is selected by configuring the TEST_MODE pin. If the Hi3520D works in normal mode, the pin must connect to a 10 kΩ pull-down resistor, as described in Table 1-2. The eFUSE pin must connect to GND through a 10 kΩ pull-down resistor.

Table 1-2 TEST_MODE pin configuration

TEST_MODE	Description
0	The Hi3520D works in normal mode.
1	The Hi3520D works in test mode.

HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

1.1.4 System Configuration Circuit for Hi3520D Hardware Initialization

The Hi3520D integrates an A9 CPU and can boot from the SPI flash or BOOTROM.

The Hi3520D is compatible with various SPI flash memories, and you can select an address mode by configuring the SFC_ADDR_MODE pin.

The JTAG pins can be multiplexed with GPIO pins by configuring the JTAG_EN pin.

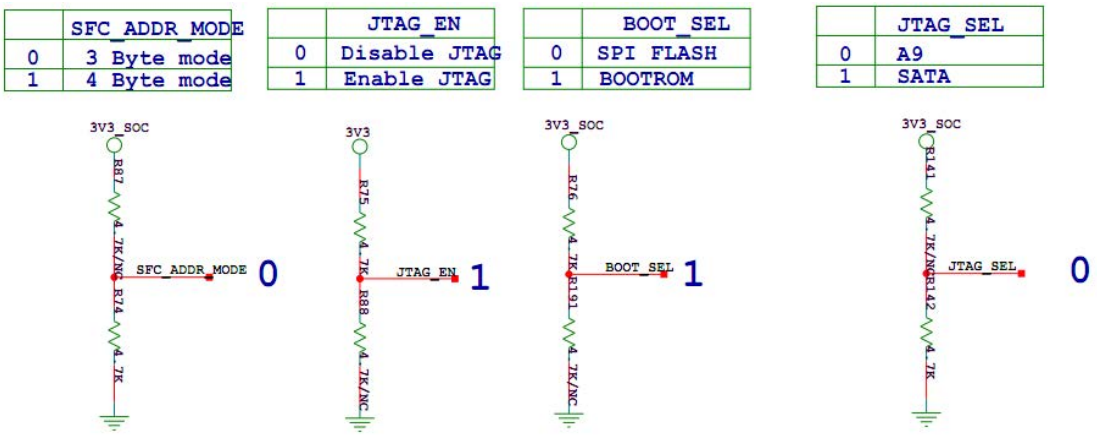
Table 1-3 describes hardware configuration signals.

Table 1-3 Hardware configuration signals

Signal	Direction	Description
BOOT_SEL	I	BOOT_SEL select. 0: The Hi3520D boots from the SPI flash. 1: The Hi3520D boots from the BOOTROM.
SFC_ADDR_MODE	I	SFC_ADDR_MODE select. 0: 3-byte mode 1: 4-byte mode
JTAG_EN	I	JTAG_EN select. 0: GPIO is selected. 1: JTAG is selected.
JTAG_SEL	I	JTAG_SEL select. 0: A9 1: SATA

The signals must be configured during Hi3520D hardware initialization. by connecting pull-up or pull-down resistors to their respective pins on the board, as shown in Figure 1-5.

Figure 1-5 Hardware initialization



HiSilicon Proprietary and Confidential
Copyright © HiSilicon Technologies Co., Ltd

以上内容仅为本文档的试下载部分，为可阅读页数的一半内容。如要下载或阅读全文，请访问：https://d.book118.com/997042100144006143